InP DHBT test structure optimization towards 110 GHz characterization

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[1] III-V Lab, joint lab between Nokia Bell Labs, Thales and CEA Leti, Palaiseau, France.
[2] IMS Laboratory, University of Bordeaux, CNRS UMR5218, Bordeaux INP, Talence, France.
[3] Nokia Bell Labs, Nozay, France

***Abstract*—In this paper, three different designs of test structures are explored in order to accurately characterize InP DHBTs up to 110 GHz. In particular, a new design, optimized for high frequency measurements while keeping high device density, has been proposed. De-embedding test structures are analyzed and InP DHBT RF figures of merit are extracted for the three designs. Extraction of the maximum oscillation frequency, f_{MAX}, confirms the relevance of optimized test structures as well as good performances of the new design.**

Keywords—Characterization, Millimeter-wave, Double heterojunction bipolar transistor (DHBT), InP/InGaAs, Indium Phosphide (InP)

I. INTRODUCTION

Due to the increase in the volume of data exchanged, developing high-speed communication systems has become crucial, be it for optical or wireless communications. For this purpose, developing transistor technologies that combine high speed and high breakdown voltage has become mandatory. InP double heterojunction bipolar transistors (InP DHBT) have these characteristics. Both Type-I [1] and Type-II [2] DHBTs have already demonstrated f_{MAX} above 1 THz while having breakdown voltages of 4.1 V and 5.4 V, respectively.

To benefit from these performances, accurate characterization of these transistors is crucial in order to confirm the high cutoff frequency and to validate the associated compact model used for integrated circuit (IC) design. Transistor characterization below 110 GHz often involves off-wafer calibration and open-short de-embedding [1]–[3]. It has been shown that measurements beyond 110 GHz are particularly difficult [4]. To perform InP DHBT characterization at higher frequencies, on-wafer thru-reflect-line (TRL) calibration has been introduced along with optimized test structures [5]–[7]. This method has demonstrated excellent results. However, it requires more area on the wafer to accommodate additional calibration structures and one needs to change the inter-probe distance during the calibration step.

However, most of these previous works do not take into account the "industrial" point of view of characterizing transistors and rather invest of developing techniques that are area consuming. With that in mind, in this paper, we introduce a new industrially compatible design. This new design contains optimized test structures as well as a high density of transistors. The rest of this paper is organized as follows: section II details the transistor technology and the three RF test structures design; section III presents the comparison of the three test structure designs on deembedding structures characterization and InP DHBT RF figures of merit extraction.

II. RF TEST STRUCTURE DESIGN OPTIMIZATION

A. Technology description

The InP DHBT structure is grown on a 3-inch semi-insulating substrate using solid source molecular beam epitaxy (SSMBE). The intrinsic emitter is 40-nm thick InP. The highly C-doped ($8 \cdot 10^{19}$ cm^{-3}) 28-nm InGaAs base is compositionally graded (from $In_{0.47}Ga_{0.53}As$ on the emitter side to $In_{0.53}Ga_{0.47}As$ on the collector side) in order to reduce the base transit time. The 130-nm thick composite collector is composed of a non-intentionally doped InGaAs spacer, a 20-nm thick highly doped layer and a lightly doped collector region. The transistors are processed using a wet-etch self-aligned triple mesa technology as described in [8]. This technology, which also includes three levels of gold metallization for interconnections, is compatible with circuit design [9], [10]. Among the characterized devices, different transistor geometries were considered: emitter width varied from 0.4-µm to 0.7-µm while the emitter length varied from 5-µm to 10-µm. Fig. 1 shows a scanning electron microscopy view of a 0.4 × 7 µm² InP DHBT.

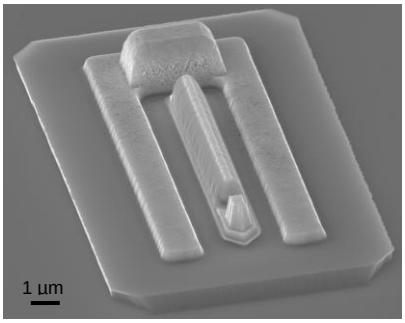

Fig. 1 . Scanning electron microscopy view of a 0.4 × 7 µm² InP DHBT before interconnection level

The performances of the 0.4 × 5 µm² InP DHBT under test have been presented in [11]. The common emitter breakdown voltage BV_{CE0} is greater than 4.5 V and the static current gain β is around 30. The transition frequency, f_T, and the maximum oscillation frequency, f_{MAX}, are 380 GHz and 605 GHz, respectively.

B. Layout and floor-plan optimization of RF test structures

In this study an optimized design of RF test structures for industrial application is proposed. In order to analyze its performances, three different RF test structures are compared. The first design is used in an “industrial” context

while the second has been designed to prove the feasibility of measurement up to 500 GHz. The third one is the new optimized design proposed in this work

1) High density pads (design 1)

This design (see Fig. 2) is the pre-defined design in standard III-V Lab process. It is designed with the purpose of maximizing the number of test structures within the chip area with different geometries of transistors. These high-density constraints are imposed due to the fact that a large number of transistors is required for process yield and variability analysis. The RF pads are compatible with 100-µm pitch probes. The density of transistor targeted with this design is 20 transistors per chip.

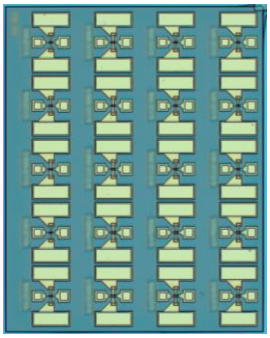

Fig. 2. Photograph of a die with high density pads

2) High quality pads (design 2)

As presented in [5], this design (see Fig. 3) combines two optimization strategies to improve the on-wafer measurement accuracy up to 500 GHz. First, a continuous ground plane was implemented in order to minimize the probe-to-substrate coupling, as well as the coupling between neighbouring structures. By connecting all the ground pads together and creating a signal pad shielding, this continuous ground plane also contributes to the improvement of the RF signal propagation along the access line. Second, on-wafer TRL calibration method was used up to 500 GHz, requiring the design of TRL standards on the same InP substrate as the devices to characterize. In addition, the RF pads were compatible with the 50-100 µm probing pitch required by the RF probes in the different frequency bands up to 500 GHz. The density of this design is 8 transistors per chip (Fig. 3 shows a chip, which has twice the area of the one in Fig. 2).

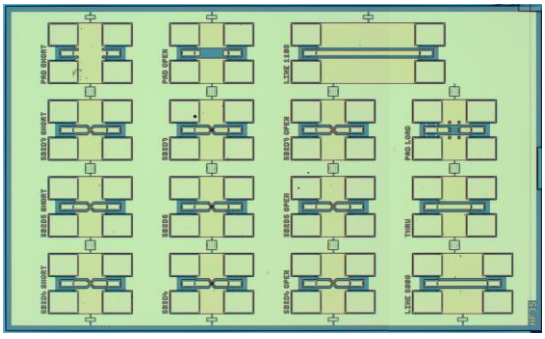

Fig. 3. Photograph of a die with high quality pads

3) Optimized pads for industrial process fabrication (design 3)

This third design (see Fig. 4) re-uses the continuous ground plane method used in the design 2 as it reduces the probe to substrate interaction for high frequency measurements. Moreover, a checkerboard configuration, as introduced in [12], was implemented. It allows the reduction of the distance between the neighbouring structures that are above and below. Thus, this configuration allows to optimize the density of test structures while maintaining a reduced coupling between neighbouring test structures. These pads are designed for 100-µm pitch probes. The density is 14 transistors per chip.

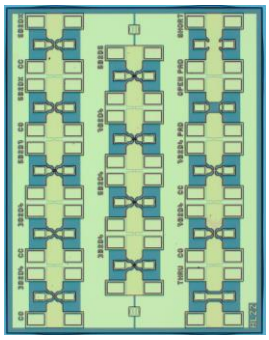

Fig. 4. Photograph of a die with optimized pads

III. Results

To analyze the performances of these three test structure designs, the measurements on a 0.4 × 5 µm² InP DHBT and on its associated de-embedding test structures were performed. The S-parameters measurements were carried out from 1 GHz to 110 GHz with an Anritsu Vectorstar network analyzer using an off-wafer Short-Open-Load-Through (SOLT) calibration and 100-µm pitch Picoprobe RF probes.

A. De-embedding test structures characterization up to 110 GHz

The accurate extraction of transistor parameters relies on a precise de-embedding of parasitic capacitances and inductances that surround the device. In order to verify the validity of the de-embedding, open and short structures are associated to electrical equivalent circuits (see Fig. 5). To verify that open capacitances and short inductances are not frequency-dependent, their values were extracted using Y and Z parameters (see Fig. 7.).

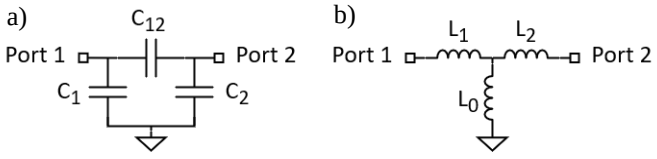

Fig. 5. Equivalent electrical circuit of (a) open and (b) short structures

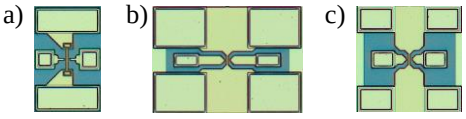

Fig. 6. Photograph of the open de-embedding structure (a) design 1 (b) design 2 (c) design 3

As observed from Fig. 7, the measured open capacitances and short inductances of the three different test structure designs are quite constant over the frequency range. There is no resonance over the 110 GHz band. Design 1 is strongly asymmetric; it explains why C_1 and C_2 (as well as L_1 and L_2) show different values. The value of C_1 and C_2 can be correlated to the metal that surrounds the signal pad, which is why capacitances of design 2 (which is designed for 50-µm probe pitch) are twice the capacitances of design 1. Moreover, for the same design, a difference between L_1 and L_2 is visible. It is caused by the different RF probe tip positioning on the pads at port 1 and port 2, resulting in an unequal distance from the center of the test structure. The sensitivity to the probe tips positioning is one of the main drawbacks of probe-tip calibration methods, such as the SOLT calibration used in this work.

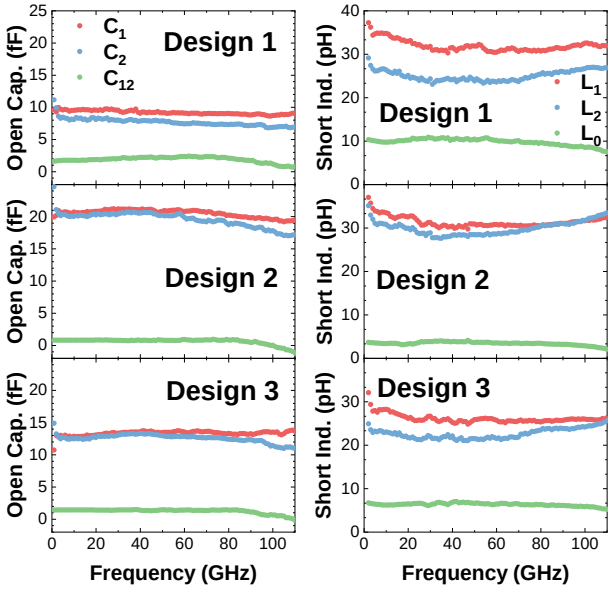

Fig. 7. Measured open capacitances and short inductances of the 3 test structure designs

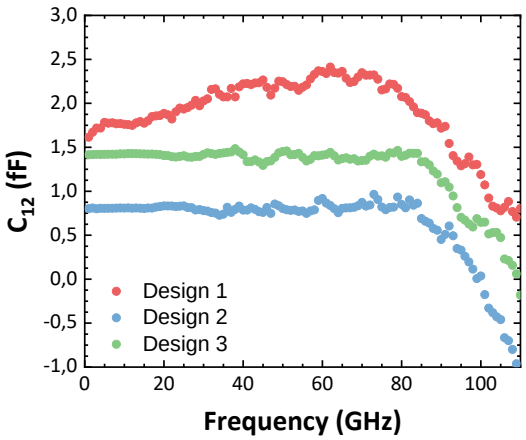

Fig. 8. Extracted port-1 to port-2 open capacitance C_{12} for the three test structure designs

Fig. 8 shows the C_{12} capacitances of the three test structure designs. It appears that in all three cases, the capacitance value starts to drop after 80 GHz. This behavior is certainly due to the signature of the Picoprobe RF probes, since it has already been observed both in EM simulation and measurement in [13], where Picoprobe RF probes were also used.

The capacitance in design 1 is not constant (up to 80 GHz), this indicates that coupling (with substrate or adjacent structures) still occurs. The probe-to-probe distance is different in the three test structure designs which explains the difference between the C_{12} capacitances values.

B. Extraction InP DHBT RF figures of merit up to 110 GHz

The InP DHBT were measured at V_{CE} = 1.6 V and different collector current densities J_C (from 0.25 mA/µm² to 9 mA/µm²). This chosen value of V_{CE} is a trade-off to combine high values of both f_{MAX} and f_T. Open-short de-embedding is performed to extract the performances of the device.

The extraction results of f_T are shown in Fig. 9. The extraction of f_T up to 110 GHz gives pretty similar results between the three designs.

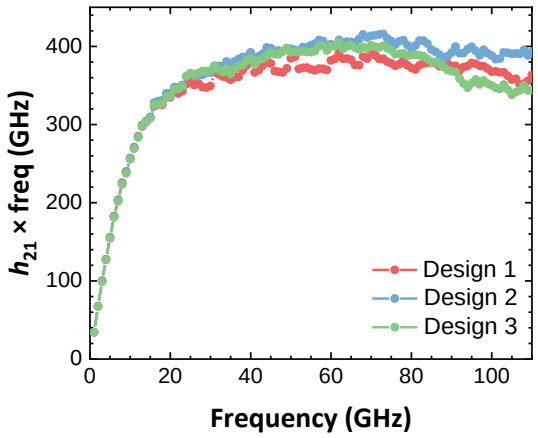

Fig. 9. Determination of f_T with gain-bandwidth product of a 0.4 × 5 µm² DHBT at V_{CE} = 1.6 V and $J_C \approx$ 6 mA/µm

On the other hand, extraction of the maximum oscillation frequency f_{MAX} is more challenging and is sensitive to the design (see Fig. 10). Design 1 leads to an inaccurate extraction of f_{MAX}, certainly due to a combined effect of crosstalk between ports and additional coupling effects for using this non-optimized RF test structure design. The industrial design 3 produces results comparable to the optimized design 2 for the extraction of f_{MAX} up to 70 GHz. This confirms the satisfying tradeoff made in design 3 between optimization of RF test structures design and high device density. The drop of the three curves after 70 GHz is attributed to RF probes (and their coupling with structures). This effect is described in [14] where probe effects appear after 40 GHz. In our case, these effects appear at higher frequencies, which is why it is still possible to extract f_{MAX} by fitting a single pole function on the measurements up to 60 GHz (as shown on Fig. 10).

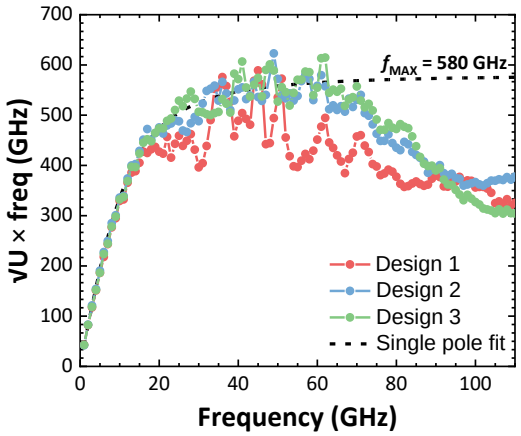

Fig. 10. Determination of f_{MAX} with gain-bandwidth product of a 0.4 × 5 µm² DHBT at V_{CE} = 1.6 V and $J_C \approx 6$ mA/µm

IV. Conclusions

Three different designs of test structures were explored in order to accurately extract RF figures of merit of InP DHBTs. De-embedding test structures were characterized and transistors RF figures of merit were extracted. The need of optimized test structures for accurate f_{MAX} extraction has been demonstrated. The new design, which maintains a high-density of transistors (1.75 times of that of design 2) while containing optimized test structures, shows similar performances as the design optimized for 500 GHz measurements (in the 110 GHz range). This work opens new perspectives to high frequency measurements beyond 110 GHz as well as accurate characterization with other RF probes.

Acknowledgment

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References

[1] J. C. Rode *et al.*, 'Indium Phosphide Heterobipolar Transistor Technology Beyond 1-THz Bandwidth', *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2779–2785, Sep. 2015, doi: 10.1109/TED.2015.2455231.

[2] A. M. Arabhavi *et al.*, 'InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With f_{MAX} = 1.2 THz', *IEEE Trans. Electron Devices*, pp. 1–8, 2022, doi: 10.1109/TED.2021.3138379.

[3] H. Xu, B. Wu, E. W. Iverson, T. S. Low, and M. Feng, '0.5 THz Performance of a Type-II DHBT With a Doping-Graded and Constant-Composition GaAsSb Base', *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 24–26, Jan. 2014, doi: 10.1109/LED.2013.2290299.

[4] K. Yau, E. Dacquay, I. Sarkas, and S. P. Voinigescu, 'Device and IC Characterization Above 100 GHz', *IEEE Microw. Mag.*, vol. 13, no. 1, pp. 30–54, Jan. 2012, doi: 10.1109/MMM.2011.2173869.

[5] M. Deng *et al.*, 'InP DHBT Characterization up to 500 GHz and Compact Model Validation Towards THz Circuit Design', in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Dec. 2021, pp. 1–4. doi: 10.1109/BCICTS50416.2021.9682466.

[6] H. Lu, W. Cheng, O. Li, Y. Kong, and T. Chen, 'Measurement and Modeling Techniques for InP-Based HBT Devices to 220GHz', in *2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, May 2018, pp. 1–3. doi: 10.1109/ICMMT.2018.8563540.

[7] D. F. Williams *et al.*, 'Calibrations for Millimeter-Wave Silicon Transistor Characterization', *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 658–668, Mar. 2014, doi: 10.1109/TMTT.2014.2300839.

[8] V. Nodjiadjim *et al.*, '0.7- µ m InP DHBT Technology With 400-GHz f_T and f_{MAX} and 4.5-V BVCE0 for High Speed and High Frequency Integrated Circuits', *IEEE J. Electron Devices Soc.*, vol. 7, pp. 748–752, 2019, doi: 10.1109/JEDS.2019.2928271.

[9] A. Konczykowska, J.-Y. Dupuy, F. Jorge, M. Riet, V. Nodjiadjim, and H. Mardoyan, 'Extreme Speed Power-DAC: Leveraging InP DHBT for Ultimate Capacity Single-Carrier Optical Transmissions', *J. Light. Technol.*, vol. 36, no. 2, pp. 401–407, Jan. 2018, doi: 10.1109/JLT.2017.2760507.

[10] R. Hersent *et al.*, '160-GSa/s-and-Beyond 108-GHz-Bandwidth Over-2-V_{ppd} Output-Swing 0.5-µm InP DHBT 2:1 AMUX-Driver for Next-Generation Optical Communications', *IEEE Microw. Wirel. Compon. Lett.*, pp. 1–4, 2022, doi: 10.1109/LMWC.2022.3161706.

[11] N. Davy *et al.*, '0.4-µm InP/InGaAs DHBT with a 380-GHz f_T, > 600-GHz f_{max} and BV_{CE0} > 4.5 V', in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Dec. 2021, pp. 1–4. doi: 10.1109/BCICTS50416.2021.9682209.

[12] M. Cabbia, C. Yadav, M. Deng, S. Fregonese, M. De Matos, and T. Zimmer, 'Silicon Test Structures Design for Sub-THz and THz Measurements', *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5639–5645, Dec. 2020, doi: 10.1109/TED.2020.3031575.

[13] M. Deng *et al.*, 'Design of On-Wafer TRL Calibration Kit for InP Technologies Characterization up to 500 GHz', *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5441–5447, Dec. 2020, doi: 10.1109/TED.2020.3033834.

[14] S. Fregonese, M. De Matos, M. Deng, D. Céli, N. Derrier, and T. Zimmer, 'Importance of Probe Choice for Extracting Figures of Merit of Advanced mmW Transistors', *IEEE Trans. Electron Devices*, pp. 1–8, 2021, doi: 10.1109/TED.2021.3118671.