A 24.25-30.5GHz Fully Integrated SiGe Phase Shifter/VGA/Power Amplifier in 0.13µm BiCMOS Technology for 5G Beamforming Applications

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***Abstract*—This paper presents a 24.25GHz to 30.5GHz wideband SiGe front-end module including a passive phase shifter (PS), a low impedance and low phase variation variable gain amplifier (VGA) and a linear power amplifier (PA) dedicated to beamforming architectures. The whole chip exhibits 33dB of maximum gain, 24dBm of saturation power (P_{sat}) and 32.5% of maximum Power Added Efficiency (PAE_{max}) at 27GHz. Phase adjustment covers 360° with a minimum resolution of 5.6° and gain covers a 16dB range by 0.5dB steps. The circuit is implemented in a SiGe 130nm BiCMOS process and occupies 0.53 mm² without pads.**

Keywords—SiGe, HBT, current mirror, phase shifter, variable gain amplifier, power amplifier, 5G, beamforming

I. Introduction

The new generations of telecommunication, such as the fifth generation (5G), require compact, reliable, affordable, and high-speed circuits. Silicon is becoming increasingly popular for power amplifiers design due to its excellent performance in terms of gain, linearity and high level of integration compared to III-V technologies. SiGe is a promising material for power amplifiers due to its combination of bipolar and MOS transistors, as well as its compact size and reliability. The integration of digital and RF circuits on a single chip is made possible through this technology.

Phase shifters (PS) and variable gain amplifiers (VGA) play a crucial role in communication systems, particularly in 5G millimeter-wave front-end using phased-array technology [1], [2], [3]. The main challenges lie in controlling the phase and the gain for the beam direction as well as reducing the side lobes. Besides this, in order to prevent distortions, the power amplifier (PA) must be driven in the linear region. The PA requires a high Power Added Efficiency (PAE) at its saturation and at 8dB of power back-off.

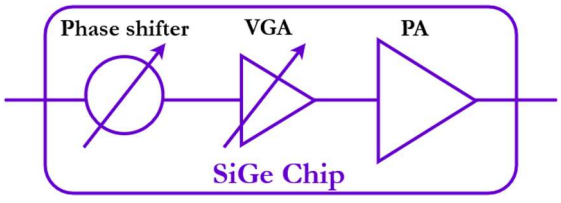

Fig. 1. SiGe mmW module including PS, VGA and PA

This paper presents the first fully-integrated RF module including phase and amplitude controls followed by a power amplifier in 0.13µm SiGe technology. Post-layout simulations are fully compliant with the mandatory specifications of the mmW 5G application. It is organized as follows. Section II describes the design of the different sub-circuits of the chip (Fig. 1). Section III presents post-layout simulations of the entire SiGe module and a comparison with other works. The SiGe chip output power is sent to a GaN HPA.

II. Circuit Design

A. Phase shifter

The phase shifter is a key element in beamforming systems. Indeed, by adjusting the phase of the signal at each antenna, the transmitted power can be directed towards a specific direction, thereby increasing the equivalent isotropic radiated power (EIRP). The quality of these systems is largely dependent on each individual phase shifter. When evaluating the performance of a phase shifter, several factors are taken into consideration including the power consumption, the insertion losses, the variation of losses regarding the phase setting, the phase resolution and the accuracy. Meeting these criteria can be a significant design challenge, especially at millimeter-wave frequencies.

In order to decrease the overall system power consumption and have a high phase resolution, the selected architecture is a Reflection-Type Phase Shifter (RTPS) [4]. It relies on passive components, resulting in zero power consumption, high linearity, and bidirectional operation. Each RTPS uses a 90° hybrid coupler and two reflective loads (Fig. 2).

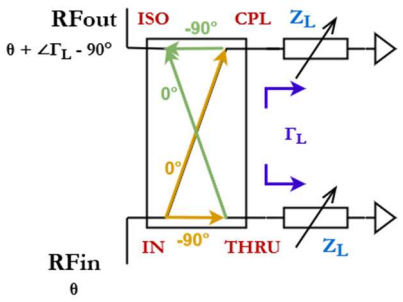

Fig. 2. RTPS principle with a 90° hybrid coupler and two reflective loads

The input signal (RFin) is separated in two signals. The first one is sent to the CPL port with a phase equal to θ. The other is sent to the THRU port with a phase equal to θ – 90°. The signal is reflected by the varactor and recombined in phase on the ISO port and out of phase on the IN port. The varactor reflection coefficient Γ_L phase enforces the phase of the signal. The phase difference between the input and the output is :

$$\Delta\Phi = \angle\Gamma_L - 90° \quad (1)$$

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By changing the capacitance of the varactor, the phase of the reflection coefficient can be changed as follows :

$$\angle\Gamma_L = 180° - tan^{-1}\left(\frac{1}{C\omega Z_0}\right) \quad (2)$$

With C the capacitance of the varactor, Z_0 the characteristic impedance. A tradeoff between $\frac{C_{max}}{C_{min}}$ ratio and the Q factor is needed. Indeed, a large $\frac{C_{max}}{C_{min}}$ ratio leads to a large phase range but a low Q factor which increases the losses. In this work, three cascaded RTPS have been used (Fig. 3).

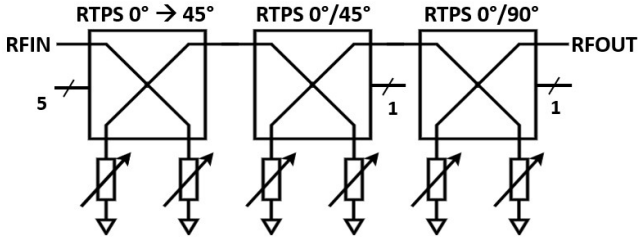


Fig. 3. Phase shifter architecture with three cascaded RTPS

The 5-bit first RTPS allows for a phase sweep from 0° to 45°, when the 1-bit second and third RTPS allow for 45° and 90° phase shift, respectively. These three RTPS together exhibit a maximum phase sweep of 180°, which can be extended to 360° using the inversion bit of the VGA (this will be explained in section B). The two first RTPS use variable capacitors called varactors and the last one is a switched capacitor.

Integrated 90° hybrid couplers are chosen for their high compactness and their low losses (0.35dB) [5] at millimeter-wave frequencies, making it possible to cascade them while minimizing the required surface area. One RTPS is composed of one hybrid coupler and two reflective loads. (Fig. 3)

RTPS1:

The first RTPS reflective load consists of five double varactors. The varactors are designed to be doubled in size for each branch. By changing the ratio of width to length (W/L), phase dynamic is changed. The varactors are independently controlled by bits *b1* to *b5*, which allows for control over the voltage (Fig. 4).

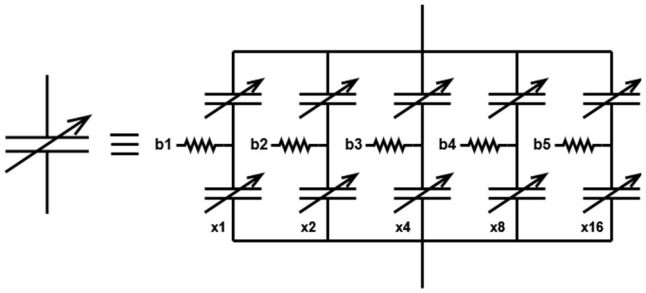


Fig. 4. First 5-bit RTPS reflective load

RTPS2:

The second RTPS reflective load features one double varactor, which follows the same design as the first one (Fig. 5a).

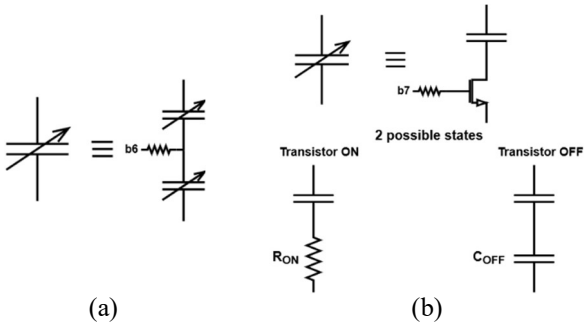


Fig. 5. Architectures of (a) the second 1-bit RTPS reflective load and (b) the third 1-bit RTPS reflective load

RTPS3 :

Reaching a phase shift of 90° with the same RTPS cannot be done with the same topology because the capacitor ratio is too large that would imply an important increase of losses. So, the third RTPS uses a switched capacitor instead of a varactor (Fig. 5b).

If the transistor is ON, the transistor is equivalent to its resistance R_{ON}. The corresponding phase is 0°. If the transistor is OFF, the transistor is equivalent to a capacitor C_{OFF}. The corresponding phase is 90°. The phase shifter layout exhibits a total size of 0.18mm² without pad (Fig. 6).

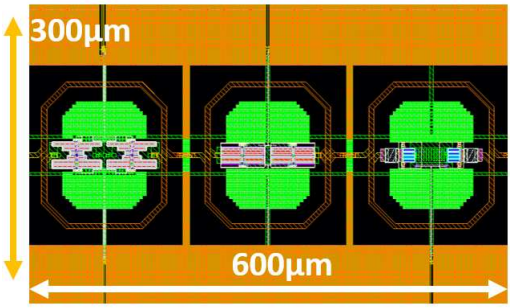


Fig. 6. Layout of the SiGe phase shifter

The drawback of this topology is that according to the binary code of the phase shifter, insertion losses are different, especially for high-order bits. To fix that, the compensation technique explained in [5] is used for the bits *b4* and *b5* which leads to put a transistor in parallel with varactors in order to smooth the losses whatever the varactor voltage.

This three-part cut of the phase shifter offers a high bandwidth, low losses, and a low variation in losses. It is the same architecture as [5] with three cascaded RTPS but every RTPS does not cover the same phase range. Indeed, in the work presented in [5], the continuous RTPS covers 60° of phase range which causes 10dB of insertion losses. In order to limit losses, it is better to reduce the range of the continuous RTPS and to complete the phase lack with the two discrete RTPS.

Post-layout results are presented (Fig. 7). The input impedance exhibits minimal variation when the binary code changes (Fig. 7a), with losses ranging from -9.5dB to -7.3dB (Fig. 7c) between 24.25 and 30.5GHz. The variation in insertion losses between all the phases is low that means there is a good EVM (Error Vector Modulator). The resolution is better than 5.6° and phases cover 180° with the phase shifter alone (Fig. 7d). A phase inversion is realized thanks to the VGA presented in section B allowing to cover 360°.

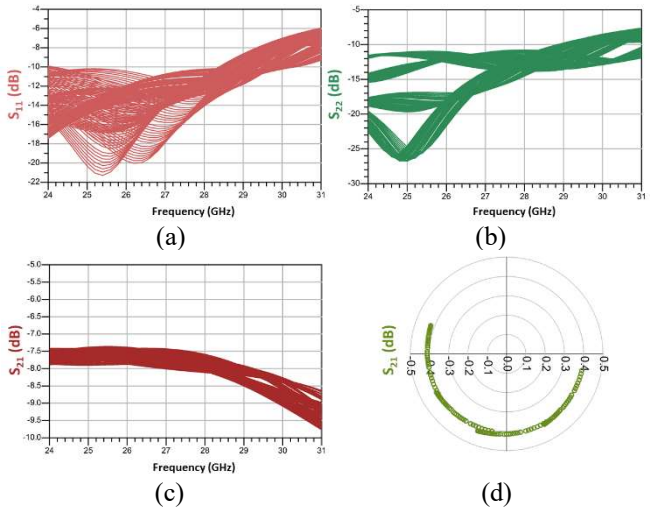


Fig. 7. Phase shifter performances with all binary codes on 24-31GHz: (a) S_{11} (dB), (b) S_{22} (dB), (c) S_{21} (dB) and (d) S_{21} covered phases at 27GHz

This phase shifter architecture, including varactors and hybrid couplers, is wideband [5]. That is important for the system to cover the targeted frequency band.

B. Variable Gain Amplifier

In order to maintain compatibility with other blocks and minimize distortion, the VGA has to offer constant input and output impedances at all gain levels. To achieve this without the need of additional calibration or compensation circuits, which can increase power consumption, device size and losses, the gain control must be precise and exhibit minimal phase variation. To further enhance the performance of the VGA and remove constraints on the RTPS, it may be beneficial to include a 180° phase inverter in the VGA design [6]. For that, the double differential architecture is used (Fig. 8). The positive point here is about the use of bipolar transistors in this RF architecture thanks to the BiCMOS technology. This allows the circuit to reach a better gain and to be more linear than with MOS transistors. Furthermore, a digital control is advantageous because it facilitates the interface with the digital signal processor (DSP) and makes the system less sensitive to environmental influences.

The current control (Fig. 8) is independent from the RF signal, and MOS transistors are chosen over bipolars due to their improved temperature variations resistance. The product $R_{ON}C_{OFF}$ of the MOS transistor, which appears like a switch in this architecture, is about 260fs. It is the same for the four cells. Simulations have been led with the same node in a CMOS SOI technology. In comparison with this technology, since the size of the transistors is small, which is the case in this work, $R_{ON}C_{OFF}$ is quite the same as for BiCMOS technology (≈ 300fs). So, for this kind of application, using MOS transistors of the BiCMOS technology gives the same performances as MOS transistors of a CMOS technology. But the advantage of the BiCMOS technology lies in the use of bipolar transistors in the double differential pair which provide better performances than MOS transistors in terms of gain and linearity.

The VGA control circuit (Fig. 8) is made up of switches and inverters, allowing for one differential pair to be active while the other is inactive [7]. This ensures that the number of transistors in use remains constant, resulting in a same power consumption regardless of the binary code. The VGA is designed to have a very small impedance variation and a low phase variation.

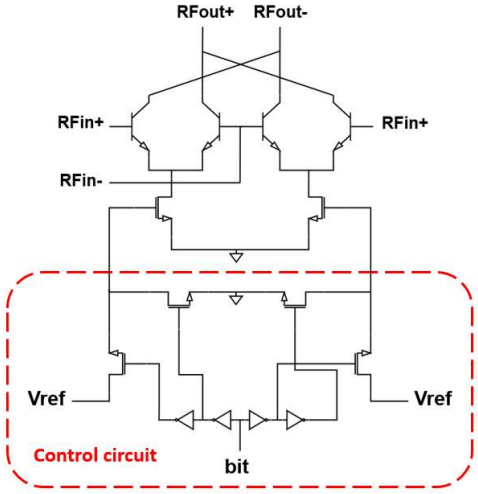


Fig. 8. VGA cell architecture with control circuit

The proposed architecture is a 4-bit digitally controlled VGA linear-in-dB. It is composed of four cells in parallel. The VGA under consideration uses switched cells for gain control (Fig. 9a). This figure illustrates that the four cells on the left are each controlled by a single bit, while the four other cells on the right are each controlled by the inverse of the corresponding bit. The symmetry of the two crossed differential pairs makes it possible to target a gain for a given phase and its exact opposite on the chart, ensuring 180° phase inversion. The transistor width of these cells is scaled enabling the gain to be linear-in-dB and precisely-defined manner using binary codes. This configuration makes it easy for a DSP to control the VGA gain. The output current of each cell is determined by the size of its transistors. The four cells correspond to four different gain levels: maximum gain (G_{max}), maximum gain minus 4dB, maximum gain minus 8dB, and maximum gain minus 12dB. To fill the gap between these stages, the reference voltage (V_{ref}) is swept from 372mV to 400mV (Fig. 9).

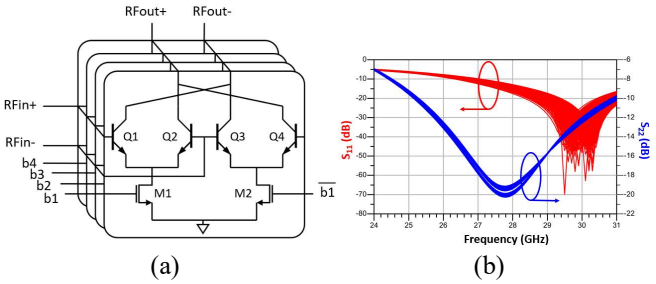


Fig. 9. VGA (a) architecture, (b) S-Parameters S_{11} and S_{22} (dB)

Bits enable a coarse sweeping whereas V_{ref} provides a fine sweeping by 0.5dB step (Fig. 10) on the 16dB range. This topology ensures low impedance variation (Fig. 9b) and minimal phase variation.

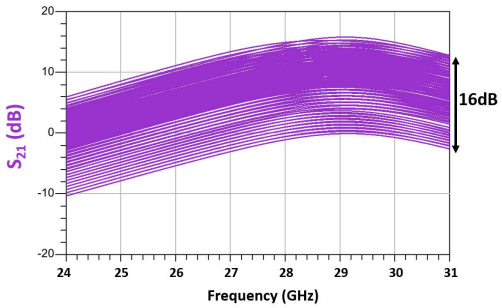


Fig. 10. 32 gain levels on 24-31GHz bandwidth

The VGA is very compact with an active area of 0.122mm² (Fig. 11).

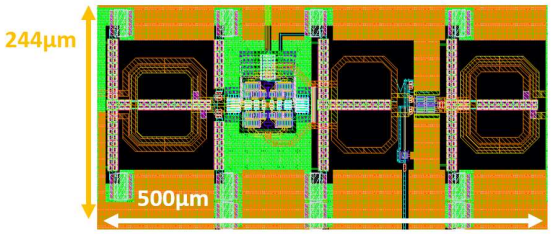


Fig. 11. Layout of the SiGe VGA

C. *Power Amplifier*

The PA consists of two stages (Fig. 12): one gain stage with a common emitter topology and a power stage with a cascode topology. The common emitter stage provides a high gain, while the cascode stage delivers the output power required in the specifications. In the cascode architecture [8], the power swing is evenly distributed between the common emitter and the common base transistors, resulting in an efficient and effective amplifier. The goal is to design an amplifier that is linear, stable, efficient at maximum power level as well as power back-off operation. To stabilize the circuit, various solutions were employed, such as RC circuits in the bases of the cascode common-emitter transistors and capacitors in the bases of the common-base transistors. Impact ionization effect, which can occur in bipolar transistors, can be counteracted by using these capacitors very close to devices. Neutralization transistors are also used to stabilize and increase the gain.

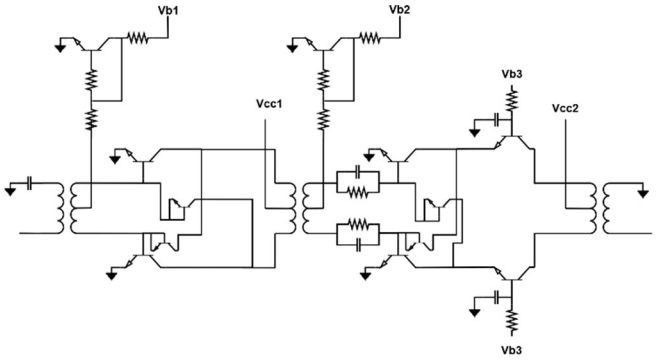


Fig. 12. Two-stage PA architecture

This project requires a circuit with a high PAE so it is essential to pay close attention to the output of the PA, particularly the output balun. This component is crucial for efficiency and consists of a single turn at the primary and secondary due to the small impedance transformation required. The output balun is 90µm wide (Fig. 13) and has a loss of 1.58dB at 27GHz. The cascode amplifier is composed of 8-emitter high-speed transistors, while the driver uses 4-emitter high-speed transistors. Dimensions have been determined by optimizing the PAE while guaranteeing enough output power [9]. Current mirrors are used to bias the bases of the common emitters in order to protect the circuit from temperature variations.

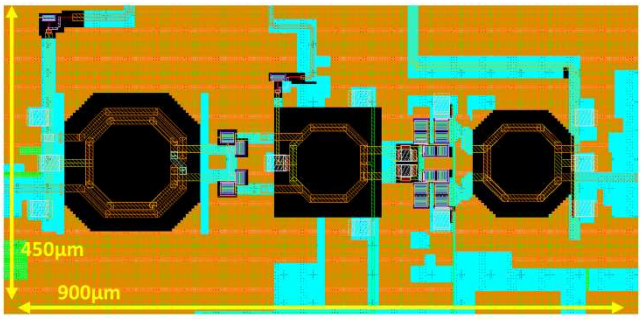


Fig. 13. Layout of the SiGe PA

The PA has been simulated at 27GHz and its performances are presented in Fig. 14. The maximum gain reaches 23.8dB and the maximum PAE reaches 31%. At 8dB of power back-off, the PAE achieves 14% (Fig. 14a). The PA exhibits 24dBm of output power at the saturation P_{sat} and 23dBm of 1dB-output compression point OCP_{1dB} (Fig. 14b). Phase distorsion is low in the linear zone (<2.2°). Fig. 14b and Fig. 14c show the good linearity of the PA. S-parameters are shown in Fig. 14d between 24 and 30.5GHz. The small signal gain S_{21} ranges from 21.1 and 24.9dB between 24.25 and 30.5GHz.

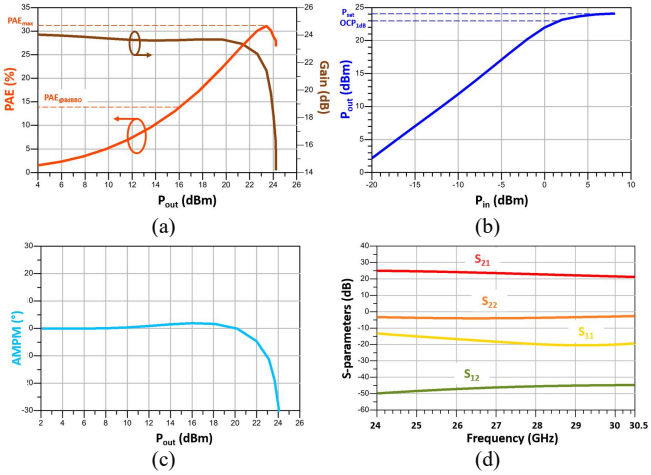


Fig. 14. PA performances: (a) PAE and gain (P_{out}) at 27GHz, (b) P_{out} (P_{in}) at 27GHz, (c) Phase distorsion at 27GHz and (d) S-parameters on 24-30.5GHz

27GHz performances have been presented but this PA provides good results on the whole band 24.25-30.5GHz. For that, passive components like baluns and transformers have been designed to be wideband. Neutralization capacitors are used to stabilize the amplifier in a broadband way. Transistors have been made to maximize the current density J_c [10] and transition and maximum frequencies f_T and f_{max}.

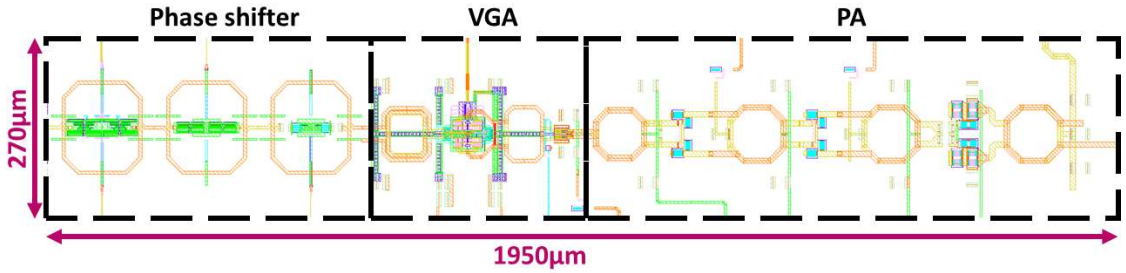


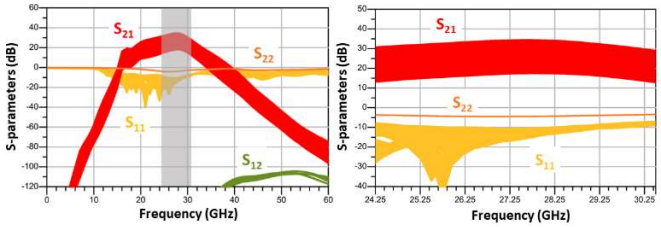
Fig. 15. Layout of the PS-VGA-PA SiGe module without pad : 0.53mm²

D. MmW PS – VGA – PA module :

To simulate the complete system including the PS, the VGA, and the PA, each block has been co-designed and transformers have been used as inter-matching networks in order to optimize impedance and reduce losses (Fig. 15). This original co-design of three blocks inside a same RF module provides very good performances in terms of beamforming and power. This front-end module is very compact (Fig. 15) and could be used in many applications thanks to its versatility.

III. Post-Layout Simulations

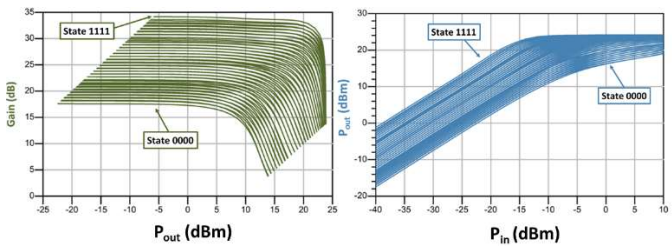
The entire chip has been simulated with all gain levels (Fig. 16). Maximum S_{21} covers 17 to 33dB on the targeted frequency band. S_{11} is below -10dB and S_{22} is below -5dB on 24.25-30.5GHz. It is easy to see on S_{11} and S_{22} parameters that whatever the implemented VGA binary code, impedances at the input and the output are the same.



(a) (b)

Fig. 16. S-parameters (a) S_{21}, S_{22}, S_{11}, S_{12} (dB) (b) S_{21}, S_{22}, S_{11} on 24.25-30.5GHz

Large signal simulations have been led (Fig. 17) and all gain levels and powers are printed at 27GHz with all possible codes of VGA bits and a sweep of V_{ref}. Power consumption (P_{dc}) remains constant (Fig. 18a) for every VGA binary code.



(a) (b)

Fig. 17. Large signal simulations of (a) Gain (dB), (b) P_{out} (dBm) ranging 32 gain levels

Maximum PAE (Fig. 18b) of the overall system is 32.5% at 27GHz for the highest gain. Fig. 18b shows that the PAE is the same for a given P_{out} whatever the code. At 8dB of power back-off, PAE reaches 14%. Fig. 18c shows the low phase variation for all VGA states at 24, 27 and 31GHz.

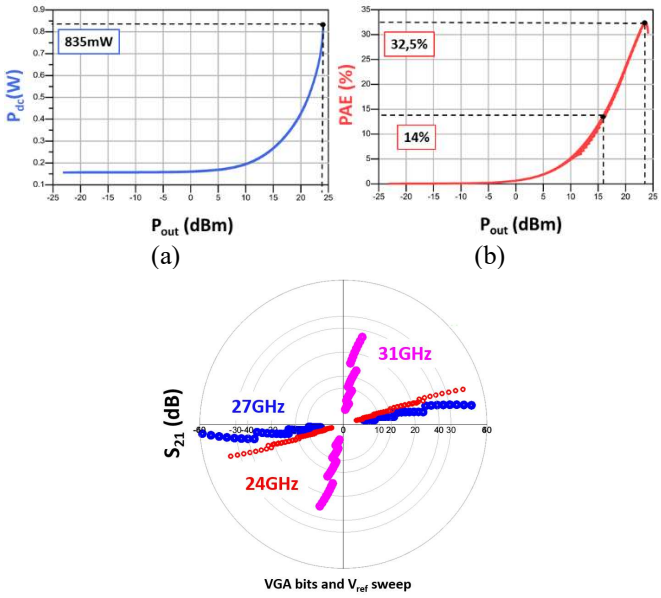


Fig. 18. For all VGA binary codes : (a) Power consumption P_{dc} (W), (b) PAE (%) and (c) Gain levels with low phase variation at 24, 27 and 31GHz

Fig. 19 illustrates the various phases encompassed by three possible VGA binary codes (and their conjugates) covering a full 360° range thanks to the VGA phase inversion bit.

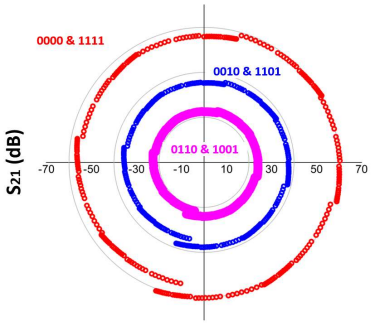


Fig. 19. Phase range with three VGA binary codes and VGA phase inversion at the RF module output

Fig. 19 shows three out of the 32 gain levels, and it is evident that the entire 360° range is covered in each of these cases.

Linear stability has been studied and is presented in Fig. 20 with the *k* factor of the same codes as Fig. 19. *k* is superior to 1 between 0 and 100GHz which proves the good linear stability of the entire chip.

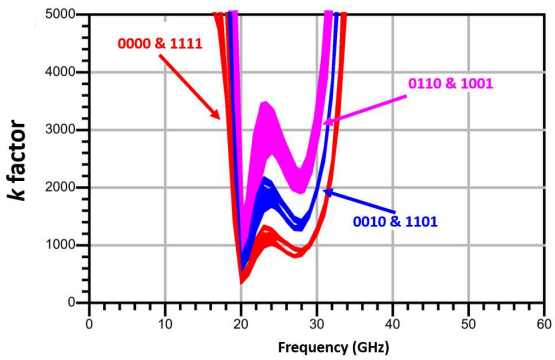


Fig. 20. *k* factor evolution between 0 and 100GHz for three VGA binary codes

The post-layout simulations results of this study are presented in Tab. I. They are compared to the results of other studies that have been measured. In terms of P_{sat}, bandwidth, PAE at 8dB of back-off, PAE_{max}, gain and phase controls, this study outperforms [1] for the same technology. In [2], the performance of a 180nm SiGe TRX module is reported, which provides a better P_{sat} due to the number of TX, but only one channel offers 12dBm of OCP1dB. According to [3], a trade-off was made between PAE and P_{sat} resulting in a higher PAE but a lower P_{sat} with the 45nm CMOS SOI technology. However, it should be noted that these results are based on four TX, unlike this study. As a result, this paper provides very compliant post-layout simulations with the mandatory 5G specifications.

IV. Conclusion

In this paper, a fully integrated module has been presented including a passive and linear phase shifter, a low impedance and phase variation VGA and an efficient and linear PA in 0.13µm SiGe BiCMOS technology. To the best of the authors' knowledges, this paper presents the best fully integrated RF module including these functions on 24.25-30.5GHz for 5G communications. The system maintains a consistent behavior across all gain levels due to the impedance being unchanged regardless of the VGA binary code. Post-layout simulations have been shown and required performances have been reached. The phase shifter allows the chip to cover 180°, the VGA brings the phase inversion to cover 360° thanks to the innovative double bipolar based differential pair. It sweeps 16dB of gain by 0.5dB step. Phase resolution is better than 5.6°. The PA enables a saturation power of 24dBm at 27GHz. Finally, the chip achieves 32.5% of PAE_{max} and 14% of PAE at 8dB of back-off. This beamformer achieves 21dBm of OCP1, 33dB of maximum gain and 17dB of minimum gain. The beamformer consumes 835mW at the saturation. The layout has been finalized and the surface of the overall circuit is 0.53mm² without pad. Even if these are simulated post-layout performances, this work provides very encouraging results regarding the state-of-the-art and its reconfigurability makes it an ideal choice for future TX 5G beamformers. Circuits manufacturing is planned for 2023.

Acknowledgement

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TABLE I. State-of-the-art

	This work (PLS)	***[1] JSSC 2017***	***[2] TMTT 2020***	***[3] CICC 2021***
Technology	**130nm SiGe**	130nm SiGe	180nm SiGe	45nm CMOS SOI
Frequency (GHz)	**24.25-30.5**	27-29	28-32	26.2-31.1
Beamforming architecture	**Analog**	Analog	Analog	Hybrid
PAE_{max} (%)	**25-33**	22*@28GHz	NA	28*-30.6
$PAE_{@8dBBO}$	**13-14**	6*@28GHz	NA	7*@29 GHz
P_{sat} (dBm)	**22-24**	16-17*	25@29GHz	20-21*
OP1dB (dBm)	**21-22.6**	13.5-15*	11-12/channel	18-20*
Phase control (°)	**360**	360	180*	180*
Phase resolution (°)	**< 5.6**	5@28GHz	5.6	1
RMS phase error (°)	**< 2.8**	0.8@28GHz	NA	NA
$Gain_{max}$ (dB)	**33**	29-32	21@29GHz	25@29 GHz
Gain control (dB)	**16**	8@28GHz	20	25*
Gain resolution (dB)	**0.5**	NA	NA	NA
Gain error (dB)	**<2dB**	0.7@28GHz	NA	NA

*estimated from curves

References

[1] B. Sadhu *et al.,* "A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications," JSSC, Dec. 2017

[2] A. Nafe *et al.,* "2 × 64-Element Dual-Polarized Dual-Beam Single-Aperture 28-GHz Phased Array With 2 × 30 Gb/s Links for 5G Polarization MIMO ", TMTT, Sept. 2020

[3] Y. Hu *et al.,* "A 28GHz Hybrid-Beamforming Transmitter Array Supporting Concurrent Dual Data Steams and Spatial Notch Steering for 5G MIMO," 2021 IEEE Custom Integrated Circuits Conference (CICC), 2021, pp. 1-2, doi: 10.1109/CICC51472.2021.9431464

[4] T. Singh *et al.,* "Compact 26–30 GHz Reflection-Type Phase Shifter With 8-Bit Switched Phase Tuning Utilizing Chalcogenide Phase-Change Switches," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 1, pp. 193-202, Jan. 2023, doi: 10.1109/TMTT.2022.3222368.

[5] S. Voisin *et al.,* "A 25-50 GHz Digitally Controlled Phase-Shifter," *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, London, United Kingdom, 2022, pp. 305-308, doi: 10.23919/EuMIC50153.2022.9783836.

[6] X. Zhang *et al.,* "A 39-GHz Phase-Inverting Variable Gain Power Amplifier in 65-nm CMOS for 5G Communication," in *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 11, pp. 1303-1306, Nov. 2022, doi: 10.1109/LMWC.2022.3180999.

[7] S. Voisin, V. Knopik, J. Forest and E. Kerhervé, "A 65 nm CMOS SOI 4-bit Digitally Controlled Variable Gain Amplifier for Ka-Band Beamforming," *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, Utrecht, Netherlands, 2021, pp. 69-72.

[8] T. -C. Tsai, C. Bohn, J. Hebeler, M. Kaynak and A. Ç. Ulusoy, "A Linear and Efficient Power Amplifier Supporting Wideband 64-QAM for 5G Applications from 26 to 30 GHz in SiGe:C BiCMOS," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Atlanta, GA, USA, 2021, pp. 127-130, doi: 10.1109/RFIC51843.2021.9490461.

[9] E. Kerherve *et al.*, "A Broadband 4.5–15.5-GHz SiGe Power Amplifier With 25.5-dBm Peak Saturated Output Power and 28.7% Maximum PAE," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 5, pp. 1621-1632, May 2015, doi: 10.1109/TMTT.2015.2415490.

[10] B. Coquillas et al., "Ku-Band Cascode Balanced SiGe Power Amplifier with High Robustness to Active SWR," 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), 2021, pp. 1-4, doi: 10.1109/NEWCAS50681.2021.9462752.