A Logic Cell Design and routing Methodology Specific to VNWFET

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Abstract—New emerging Vertical NanoWire Field-Effect Transistors (VNWFET) appear promising for compact energy efficient computing architectures, still, we notice a lack of technology aware and coherent design methodologies. Such tools would enable a thorough exploration of the benefits of these new technologies at the circuit level. This paper explores a complete methodology for designing a logic cell library using VNWFET. The methodology includes low-level logic cells Technology Computer Aided Design (TCAD) simulations, Parasitic Extraction (PEX) of predictive devices and 3D physical design rules and cell generation.
In this design method, we focus on the standard CMOS logic cells, with up to 12 transistors and detail the inter-transistor routing. The various cells generated using this method are tested using TCAD and selected based on their PEX results. The whole process is performed on logic cell examples and in the light of the current design context, results show an improvement in footprint area optimization.

Index Terms—VNWFET, junction-less, logic cell, routing, predictive, simulation, technology, TCAD, Manhattan.

I. Introduction

With today's new trends in nano-electronic devices, we witness new types of transistor architectures. The studied technology in this work, Vertical NanoWires Field-Effect Transistors (VNWFET), exhibits a native 3D structure and a vertical junction-less channel on which vertically stacking gates is possible. Considering these fundamental differences in device structure, we question the current design methodologies and their readiness regarding those new technologies. The methodology we are exploring in this paper is applied specifically to VNWFET, a technology introduced in [1] and previously studied in [2]. This footprint optimization process will be accompanied by a TCAD assessment of the generated structures in order to minimize electrical parasitics and constitute a co-optimized standard CMOS cell library.

II. Vertical NWFET technology

Based on previous work [2], where the authors use a technology specific compact model described in [3] and demonstrate the electrical design of CMOS standard cells using VNWFET. Our goal in this article is to prepare a physical design methodology specific to this same technology using a custom 3D modelling tool.

A. Advantages of junction-less transistors

In 2010, a pioneering publication [4] presents a junction-less device manufacturing process and characterisation. In fact, current junction-based transistors are a manufacturing challenge when reducing the device dimensions. Current sub-10nm technology nodes require very abrupt doping concentration changes that are challenging to manufacture, even for the most advanced foundries:

"...from n-type with a concentration of $1e^{19}cm^{-3}$ to p-type with a concentration of $1e^{18}cm^{-3}$ in a couple of nanometres ." [4]

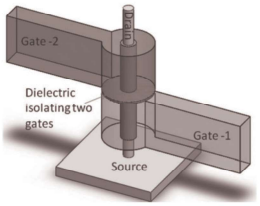
Added to this precision challenge, the charge carrier diffusion within such a junction needs to be prevented with high-speed and high-temperature annealing processes [5]. With our VNWFET technology, we not only have a very precise control of gate length but we also are not limited by junction exigence in our channel. This aspect of vertical junction-less devices is also noticed by large research groups such as IRDS [6] [7] and given high hopes. Given this notion and backed up by previous articles focused on the same technology [2] [3] [1] [8], we will

* Work supported by the LEGO project,
ANR funding (Grant ANR-18-CE24-0005-01).

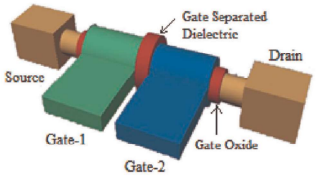
explore implementations of two stacked gates transistors in parallel with the single gate devices.

B. Stacking gates

Using multiple gates on the same nanowire channel is commonly called Parallel Gates (PG) transistors as in [9] where both gates are controlled separately to perform electrical doping along the channel. Unfortunately, this article focuses on transistors with channel junctions which is not the case for our technology. Nevertheless, it is interesting to observe the electrical behaviour of this structure as shown in Fig. 2 and recognize a Boolean function pattern.

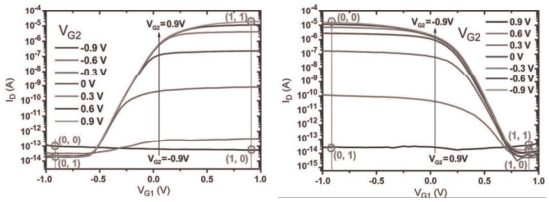


(a) Studied device representation extracted from [9]



(b) Studied device representation extracted from [10]

Fig. 1: Parallel gates transistor devices studied in two separate articles.



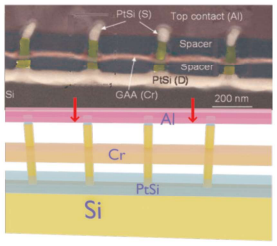
(a) nmos PG transistor (b) pmos PG transistor

Fig. 2: Parallel gates transistor characteristic according to both gates voltages. These figures are extracted from [9]

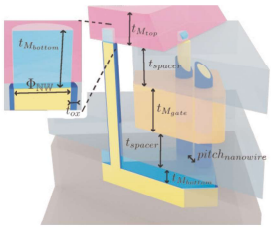
Indeed, if we focus on n-type transistors, we observe a consistent behaviour between the vertical device shown in Fig. 1a studied in article [9] the horizontal device shown in Fig. 1b studied in article [10]. Although these devices exhibit an important manufacturing difference such as the channel orientation and the doping distribution, similar logic behaviours emerge from both parallel gates controlled devices. Based on these results, we can safely assume stacking gates on our junction-less devices is comparable to two transistors in source-drain connection.

C. Structure representation

In the finished device from [1] pictured in Fig. 3a and modelled in 3D in Fig. 3b, we can highlight the various elements enabling the resulting structure to be considered a transistor.



(a) MEB image from [8] showing the cross section of a vertical nanowires transistor.



(b) Perspective and cut view of a modelled VNWFET transistor with its essential manufacturing constraints.

Fig. 3: VNWFET structure and manufacturing context.

D. Visual simplifications

In order to increase visibility in further representations, the insulating spacers will not appear thus leaving enough room to focus on the important structural details such as the metal contacts or the nanowires. Similarly, to facilitate the differentiation between p- and n-type, the remainder of this paper will not display the gate oxide surrounding the silicon nanowire either. Moreover, since we value the lateral footprint of our cell over its height for performance estimation, vertical dimensions are not to scale for the representations we use in order properly distinguish separate layers when studying a structure.

III. Non-Manhattan routing

How transistors are routed together has not really been questioned, most circuits today are essentially using "Manhattan" routing styles. This routing style consists in horizontal or vertical succession of rectangles to link transistors together, prohibiting any angle smaller than 90° to appear. While this "Manhattan" routing style makes sense, has been proven and simplifies the place and route algorithms available and manufacturing, article [11] explores the possibilities of an alternative routing scheme for logic cells.

A. Limitations with VNWFETs

Given the vertical stacking of the source, drain and gate contacts, we are forced to overlap metal contacts around the nanowire. When manually routing CMOS cells with VNWFET technology, introducing offset to transistors positions gave an advantage in terms of compactness.

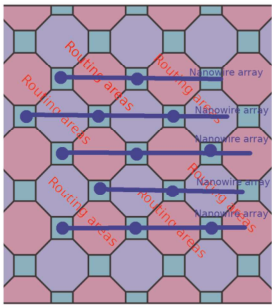
Moreover, if we restrict ourselves to a Manhattan style routing, straight angled routes crowd the available surface forcing us to place the transistors further apart and add vias. It is also important to point out that this tendency for interconnect congestion increases with the number of stacked gates.

B. The truncated square tiling

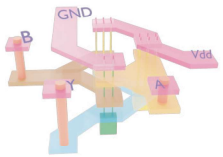
When allowing ourselves freedom regarding routes orientation, even though we risk generating a lot of complexity in the design, we may avoid overlapping metal routes

and improve cell compactness. This observation calls for a compromise between manufacturing compatibility and compactness of the cell at the design stage.

Based on the previous considerations, we chose a particular tiling for our transistors that will enable us to introduce offset to the placement while restricting the routing to a few simple repeatable structures and not introducing angles smaller than 45°. The tiling introduced in [11] is shown on Fig. 4a, we show in blue the planned positions for the transistors or vias, meaning diagonally placed squares. Given a constant spacing between each square, the remaining area in octagones is used for linking those elements together. Along with its increased flexibility for routing directions, allowing us to connect a transistor with 8 of its neighbours, all segments that constitute the floor-plan pattern (Fig. 4a) have the same length we call Γ.



(a) Choice of tiling for designing our logic cells



(b) Parasitic optimized NAND cell using two stacked gates (JL2) and an octilinear routing

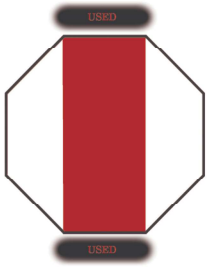
Fig. 4: Truncated square tiling as a floor-plan basis for octilinear routing

It is also important to note that the truncated square floor-plan we use is defined by a single parameter being the length of any side of either a square either an octagon. Moreover, the allowed routing angles are never smaller than 45° and the surface of transistor reserved area constitutes around 20% of the total floor-plan.

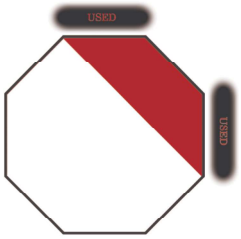
C. Generating octilinear routes

The introduced complexity of this routing remains low, infact, we can perform all routing using a few shapes. By construction, the two basic elements we can encounter are represented in Fig. 5. Based on the octilinear routing floor-plan, we can translate our routing process between two transistors into an place and route optimisation problem. By listing the common octagons for the two transistors we want to connect and whether or not the connection happens on the same layer, we are able to distinguish three characteristics of an individual link:

1) The vertical position (layers) of the two edges of the link
2) Are the transistors sharing a common octagon of the floor-plan in their direct vicinity.



(a) Straight link through the routing octogone

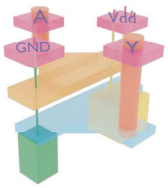


(b) Angle routing on a side of the routing octogone

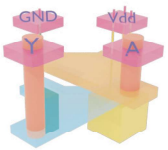
Fig. 5: Basic elements for routing inside octogone, the «USED» sides are a marker for a square that belongs to the red colored network.

3) The relative position of the transistors on the wafer plane

From there, we choose to generate a large number of possible routing by introducing randomness in the place and route algorithm, thus allowing us to generate a large panel of valid logic cells. As a result, for a simple CMOS inverter, we obtain the two circuits represented in Fig. 6, these circuits are represented with vias at their interfaces to bring the outputs and inputs to the top contact layer.



(a) Version 1



(b) Version 2

Fig. 6: 3D representation of a CMOS inverter using the octilinear routing style and our VNWFET technology

IV. Creating a cell library

Now that the inter-transistor routing methods are detailed and illustrated for a simple logic cell, we can explore device generation for a large choice of different logic cells. Our goal is to generate the basic CMOS standard cells in different technology variants (given by the number of stacked gates or the routing style) and assess the performance of those cells.

A. Assessing the octilinear routing performances

We decided to focus on 4 CMOS cells : the inverter, NAND, NOR and XOR gates following two routing styles, the octolinear (our method) on the one hand and the classical Manhattan style on the other hand. Moreover, the library generation is carried out on single gate vertical transistors (JL1) and two stacked gates transistors (JL2). This results in almost 30 different generated cells given that their are multiple generated variants for half of the

structures following the octilinear routing. As a technology agnostic approach, the footprint is expressed in Γ^2 (the base unit introduced in section III.B for both routing styles. Using these results, we first notice a general trend where JL2 devices never display higher footprints than their JL1 equivalents. Also, neither the inverter nor the Manhattan routing cells change their footprint areas when adding a second vertical gate (moving from JL1 to JL2). For the inverter, this is easily observable from its 3D representation Fig. 6a, considering the hypothesis of Section II.B, there is no need for two transistors of the same type in series in such a cell thus no optimization possible when stacking gates.

Regarding the Manhattan routing style, when creating the design, we notice that all the space gained from reducing the number of transistor footprints is lost to interconnect congestion. This was expected, as explained in Section III.A, due to the limited number of output directions that may cause metal overlapping or via necessities.

B. Scalability of routing methods

We can also put in comparison those obtained footprint values by using the number of transistor per logic cell as a parameter for footprint area as in Fig. 7.

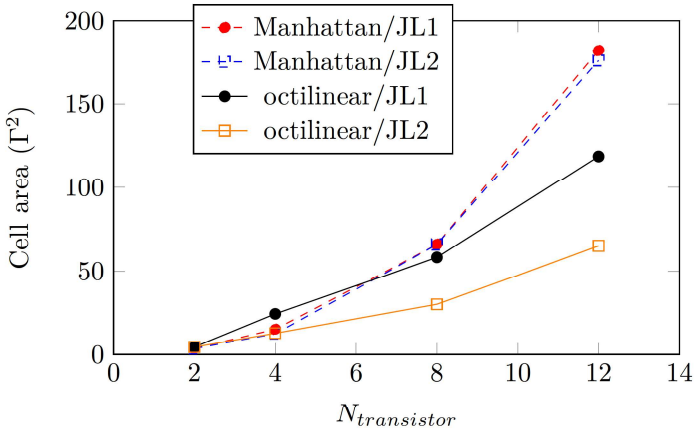


Fig. 7: routing style comparison

We notice very specific trends giving a good hint on the scalability of the octolinear routing style with VNWFET compared to the Manhattan style. The space gained by stacking transistor leads to a higher interconnect congestion and this plays better with octilinear routing offering more output directions.

V. Parasitics optimization

With modern tools, Technology Computer Aided Design (TCAD) simulations enable a precise electrical performances estimation on nanoscale devices, this greatly improves the prototyping of novel logic designs.

A. Running TCAD simulations

During this work, we were able to project our designs in a high-end manufacturing context and assess precisely their electrical behaviour. We ran TCAD simulations using GTS tool [12] on several variations of the NAND design in octolinear routing and compared the parasitic contribution in cross-net fringing capacitance. Using our modelisation tool, we were able to generate gds masks for our designs as well as a technology file and feed them into the TCAD simulation software. As a result, we obtain parasitic capacitance estimation between each network of the logic cell allowing us to draw comparison between various envisioned structures.

B. Simulation results

In the Fig. 8, the data is arranged in certain manner to gain compacity. A single bar is infact a sum of cross-net parasitic capacitance on a given net, each contribution is color coded and appears in the legend. Furthermore, net to net interaction forces us to display data path along two dimensions, this is why the x axis gathers multiple groups of bars, each corresponding to a net in symmetry with the color code. Finally, each group of bar contain as much elements as there are studied structures, 5 in our case for the octilinear style NAND cell.

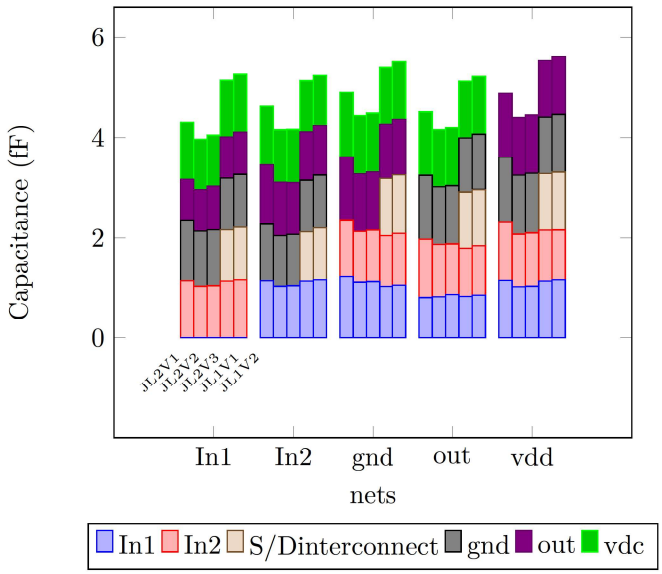


Fig. 8: For each net configurations of a NAND cell 1 to 5 are shown in parallel. The three first configurations are 2stacked gates technology (JL2V1, JL2V2, JL2V3) while the last configurations are single gate technology (JL1V1, JL1V2). For the two JL1 configurations, an additional interconnect capacitance (S/D interconnect) is measured.

From the histogram Fig. 8, we can see that considering any of the net, the JL2V1 structure exhibits the lowest parasitic capacitance. And that regardless of the version

of the cell, JL1 technology exhibits higher parasitic capacitance than JL2 technology. Going back to Section III.C where we generated multiple cells for a single boolean function, we are able to choose the most electrically efficient cell, thanks to TCAD simulations. In the case of the NAND cell with two stacked gates, we can visualize its implementation in Fig. 4b.

VI. Conclusion

In this paper, based on current interconnect congestion concerns in nanoscale devices, we investigated new methods for linking our VNWFET devices and created novel logic cell structures optimized using TCAD. We first introduced our technology based on our previous work and detailed how such devices may allow industry to push past current manufacturing limitations and move to vertically integrated devices. Secondly, we demonstrated the potential footprint area reduction such methods can offer, especially when scaling the number of transistors or moving to parallel gates technologies. These results were obtained with consideration of the manufacturing complexity introduced by these exotic routing methods. After having introduced our routing methodology and generated multiple versions of a single logic cell, we used a TCAD simulation tool to select the best candidate for a given Boolean function. A CMOS library constituted this way ensures a strong basis for designing complex logic circuits with co-optimized footprints and electrical behaviour.

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