Combination of selective area sublimation of p-GaN and regrowth of AlGaN for the co-integration of enhancement mode and depletion mode high electron mobility transistors

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ABSTRACT. We report on the fabrication of an enhancement mode p-GaN/AlN/GaN high electron mobility transistor with selective area sublimation under vacuum of the p-GaN cap layer. The GaN evaporation selectivity is demonstrated on the thin 2 nm AlN barrier layer. Furthermore, the regrowth of AlGaN is a major key to increase the maximum drain current in the transistors and enables the co-integration with depletion mode devices.

Keywords: HEMT, GaN, selective sublimation, regrowth.

Highlights:

- Selective sublimation of p-GaN is developed to fabricate enhancement-mode HEMTs
- AlGaN regrowth drastically reduces access resistances in enhancement-mode HEMTs
- Sublimation and regrowth are combined to co-integrate E/D-mode GaN HEMTs

Introduction

Gallium nitride (GaN) is a wide bandgap semiconductor of choice for high-power and high-frequency applications thanks to its outstanding material properties (high breakdown voltage, high electron velocity and good thermal conductivity [1]. The standard AlGaN/GaN High Electron Mobility Transistor (HEMT) device is a depletion-mode (D-mode) transistor and to date, the main success of GaN electronics relies on this kind of devices [2-4]. However, enhancement-mode (E-mode) transistors are required for several applications: first for safe power switch applications [5], second for the co-integration with E-mode devices for high-frequency analog and digital applications where they help to simplify the design of circuits [6-7]. Yet, an efficient way to shift the threshold voltage is to perform a gate recess or to introduce an additional layer such as a p-doped GaN cap on top of the barrier layer [8] to be removed from the device access regions. However, such layers are chemically stable and plasma-based etching is required with the drawbacks of possible degradation at the surface of the barrier layer. To overcome this problem, we have developed an innovative process based on the selective evaporation under vacuum (sublimation) of GaN [9-10]. We have shown that a dielectric mask can be patterned to define the region where GaN sublimates. Local evaporation of the p-GaN cap layer can be obtained in the access regions of the enhancement mode transistor with micrometric gate patterns. On the other hand, the D-mode HEMT devices are fabricated in other areas from where the p-GaN layer is removed.

So the E-mode and D-mode devices are co-integrated on the same substrate. In this way, we have demonstrated the co-integration on the basis of a GaN-on-Silicon HEMT structure composed of a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier layer and a 50 nm p-GaN cap [10]. Even though the threshold voltage was successfully shifted from Vgs=-1V to Vgs=+0.5V the maximum drain current in the E-mode and D-mode transistors remained around 0.18 and 0.35 A/mm respectively at V_{gs}=+2V, as a result of the trade-off necessary when the barrier is kept unchanged. The AlGaN barrier doesn't sublimate under vacuum at temperatures below 1000°C, which is an advantage for the selective evaporation of the p-GaN cap, but this constitutes also a limitation of this approach. To tackle this issue, we propose to combine the selective evaporation of p-GaN with a regrowth step of an AlGaN layer. The interest of the regrowth of AlGaN has been shown earlier for obtaining a larger carrier density and then a reduced resistance in the access regions of E-mode HEMTs made with thin AlGaN barriers [11-12]. It has also been proposed to fabricate MOSFETs with lower access resistances [13]. In the present work, not only the combination of AlGaN regrowth with p-GaN evaporation is proposed to reduce access resistances in the E-mode HEMTs, but also it allows the fabrication of D-mode devices co-integrated within the same process.

II. Experimental

The initial structure was grown by molecular beam epitaxy (MBE) with an ammonia source in a Riber Compact 21T system. The epi-layer of this structure consists of an AlN/AlGaN/AlN stress mitigation stack nucleated on a 2 in. Si(111) substrate, a 1.5 µm GaN buffer, and a 2 nm AlN barrier. As described in ref. 10, a 50 nm GaN cap p-doped with Magnesium was regrown in another MBE reactor with a nominal acceptor concentration of Na-Nd~$3.5x10^{18}/cm^3$.

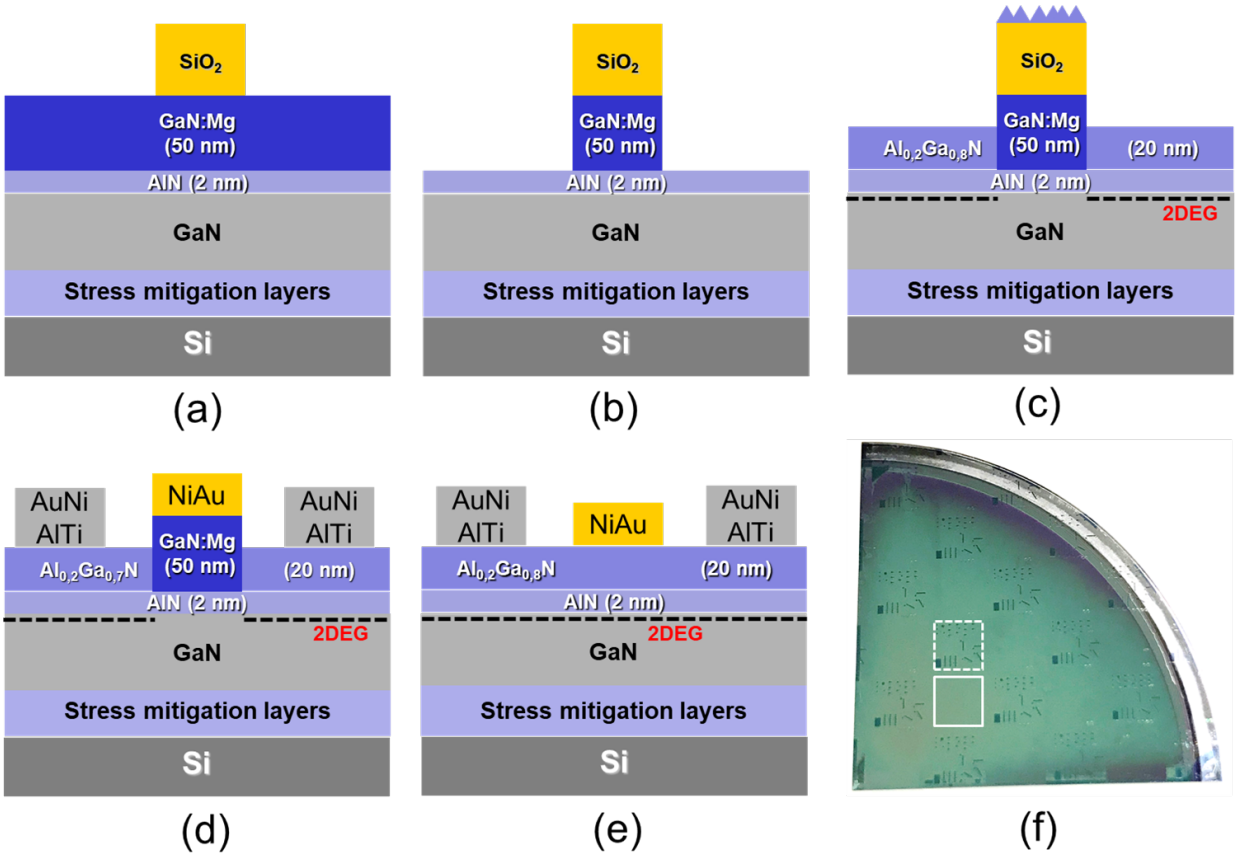

Figure 1. Schematic cross section of the fabrication. (a) initial epi-layers covered with SiO_2 and patterned; (b) selective evaporation of p-GaN cap; (c) regrowth of AlGaN; (d) E-mode transistor; (e) D-mode transistor; (f) photograph of the quarter wafer with SiO_2 patterned for E-mode transistors (area defined by a dashed line) and D-mode devices (area defined by a continuous line).

As first processing step, a 100 nm thick SiO_2 mask was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) and the substrate was cut into pieces to develop the mask patterning and sample cleaning prior to selective evaporation. One quarter of the wafer was then processed for selective evaporation and AlGaN regrowth as depicted in Figure 1. The mask patterning and evaporation of p-GaN was achieved as described in ref. 10. The AlGaN regrowth step was performed at 800°C using standard growth conditions used for AlGaN/GaN HEMTs [14]. This regrowth step was performed in the same reactor, immediately after p-GaN sublimation in order to avoid any oxidation of AlN. The SiO_2 mask was removed in a buffered oxide etchant (BOE 7:1) solution. The wide gate device process was achieved with UV-photolithography. Isolation was performed with reactive ion etching (RIE) of a 150 nm depth mesa using a $Cl_2/Ar/CH_4$ gas mixture. Ohmic contacts were formed after deposition of a Ti/Al/Ni/Au sequence in an e-beam evaporator followed by thermal annealing for 30s at 750°C in nitrogen atmosphere. The gate contact consists of a Ni/Au metal stack evaporated on p-GaN for enhancement mode (Fig.1.d) and on regrown AlGaN for depletion mode devices (Fig.1.e). Finally, an additional Ni/Au sequence was deposited on the pads of the gates as well as on the ohmic contacts to facilitate electrical measurements. I(V) measurements were performed with 2400 Keithley Source-Meters. The devices are not passivated.

The lateral width of the transistors is 150 µm. Scanning electron microscope pictures of the E-mode and D-mode devices are shown in Figure 2.a and Figure 2.b respectively. The line-edge roughness around the p-GaN region is due to the photolithography and the etching of the SiO_2 mask. For this study, the maskset was designed in order to generate a p-GaN pattern width larger than the one of the metal Schottky gate (Figure 2.a). Nevertheless, the main difficulty remains to realign the gate metal pattern on the p-GaN pattern. Gates are centred between source and drain ohmic contacts. The nominal gate lengths are 1 µm, 2 µm and 3 µm but our lithography process is not able to reproduce such dimensions and results in wider gates. As shown in Figure 2, the process of nominal 1 µm gate length and 10 µm source to drain spacing results in 1.5 µm gates inside 9.5 µm source to drain spacing.

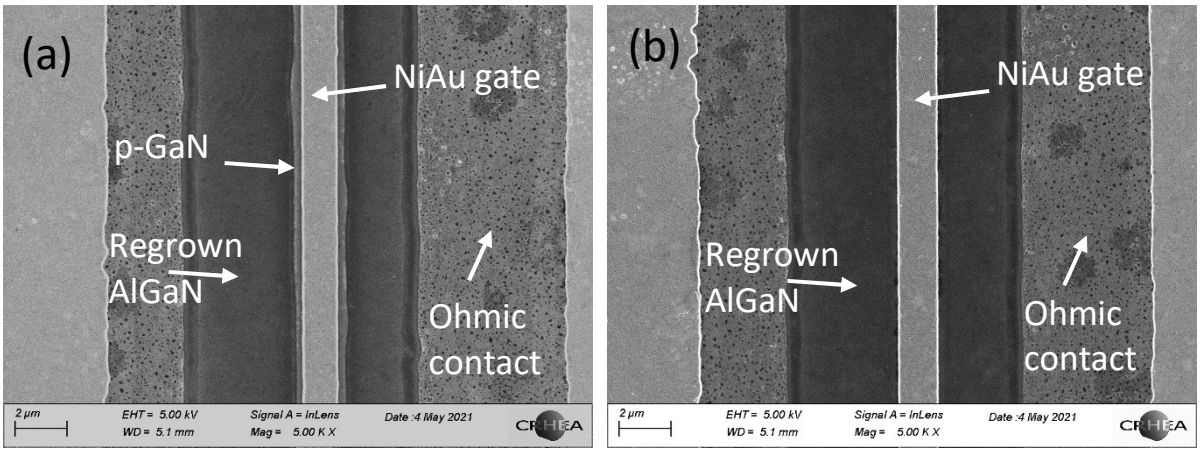

Figure 2. Scanning electron microscope views of the (a) E-mode and (b) D-mode transistors.

Results and discussion

The surface of the HEMT sample in the vicinity of the gate pattern was characterized with tapping mode atomic force microscopy (AFM). Figure 3 shows surfaces with the typical morphology of GaN layers grown with ammonia source MBE which consists of mounds with a typical diameter of 1 µm resulting in a root mean square roughness (RMS) below 5 nm [15]. This morphology doesn't affect the electron mobility of the two-dimensional electron gas (2DEG) as shown in our previous studies [10,14]. The height profile confirms that at the edges of the gate pattern the 50 nm step generated by the evaporation of the p-GaN cap layer is reduced to about 30 nm due to the regrown $Al_{0.2}Ga_{0.8}N$ barrier layer. The regrowth of AlGaN is not totally selective with respect to the SiO_2 mask which has to be sufficiently thick to enable the lift-off of crystallites nucleated on it (Fig.1.c). The presence of some spots on the image is due to an incomplete cleaning of the sample after the SiO_2 removal with BOE.

The surface of the 2 nm AlN layer revealed after p-GaN evaporation was studied on another sample used for patterning optimizations [10]; the latter presented an RMS roughness around 3 nm. Fig.3.b shows the surface with unchanged morphology after the regrowth of the $Al_{0.2}Ga_{0.8}N$ barrier layer. Pits corresponding to the emerging dislocations are clearly identified with a density estimated to a few 10^9 /cm².

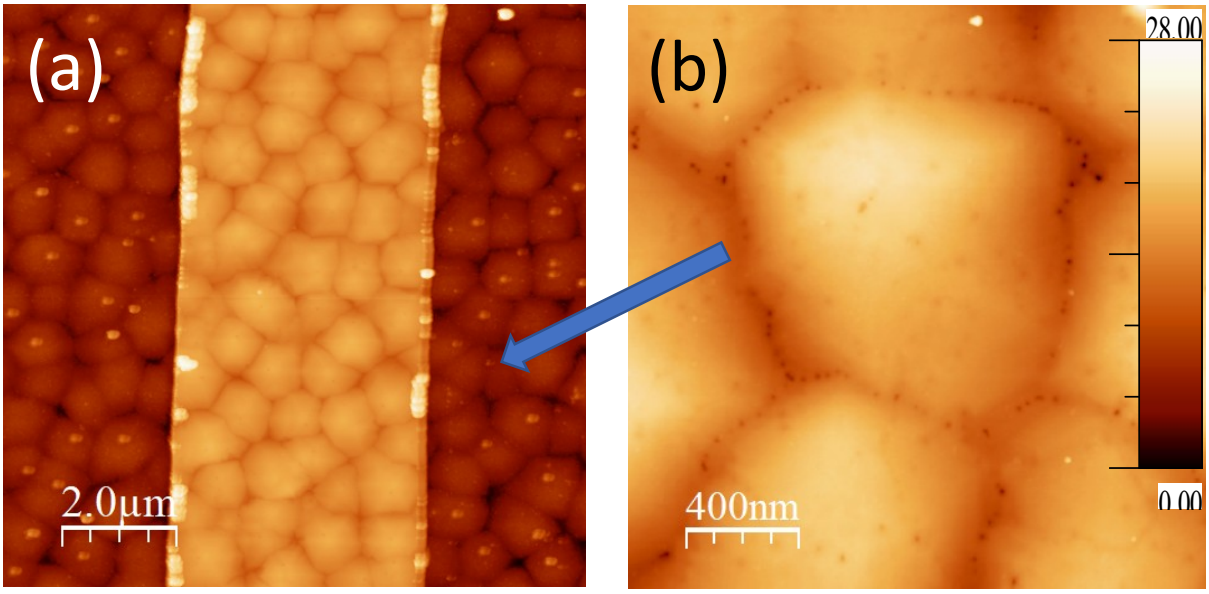

Figure 3. (a) AFM view of the gate region after p-GaN evaporation, AlGaN regrowth and SiO_2 mask removal. (b) AFM view of the surface of the regrown AlGaN.

Hall effect measurements performed on Van der Pauw cloverleaf devices confirm the sheet resistance values around 400 Ohm/sq associated with a 2DEG sheet carrier concentration greater than $1.1x10^{13}$/cm² and electron mobility above 1100 cm².V.s. Such a carrier density is much higher than the $5x10^{12}$/cm² obtained in the frame of our previous study where a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier layer HEMT without the 2 nm thick AlN layer was grown [10]. It may appear as a bit large considering the total barrier structure (20 nm $Al_{0.2}Ga_{0.8}N$/ 2 nm AlN). This may be due to the contribution of Si impurities coming from the SiO_2 mask [16] and acting as additional donors at the regrown interface. The transmission line method (TLM) was used to evaluate the ohmic contact resistance on the regrown areas. The contact resistance is below 0.3 Ohm.mm. It is a noticeable progress compared to the 0.5 and 1.7 Ohm.mm obtained previously on HEMTs with 15 nm $Al_{0.26}Ga_{0.74}N$ barrier and 2.5 nm AlN barrier respectively [10]. This is probably due to the higher electron density that helps to reduce the contact resistances.

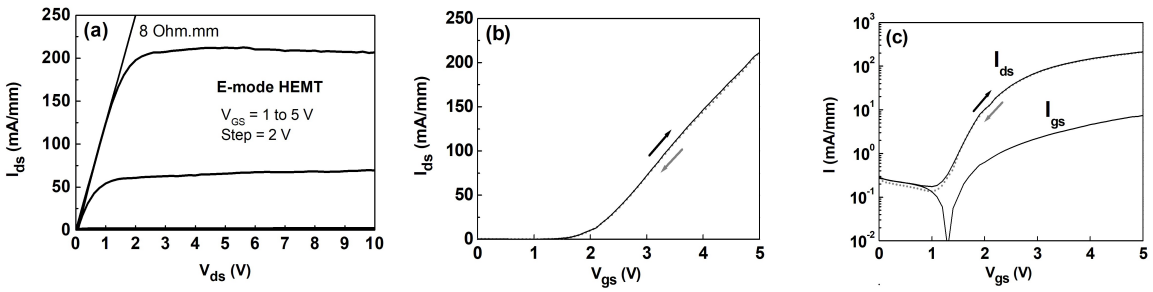

Figure 4. (a) DC output characteristics of a 1.5 µm gate E-mode transistor. (b) Hysteresis transfer characteristics V_{ds} = 7V. Solid line shows I_{ds} for positive sweep of the gate bias; dashed line represents

I_{ds} for negative sweep of gate bias. (c) Log plot of the drain current I_{ds} and the gate current I_{gs} recorded in the same conditions.

The DC output and transfer characteristics of an E-mode transistor are shown in Figure 4. The threshold voltage V_{th} defined for I_{ds}=1 mA/mm is greater than 1.5 V. The total resistance R_{on} extracted from the slope of the linear region of I_{ds}-V_{ds} curves is around 8 Ohm.mm. We have to remind that without the regrowth of AlGaN, the 2 nm AlN HEMT is depleted of electrons with a sheet resistance of about 1 MOhm/sq. This is consistent with other work [17] in which the threshold voltage is reported around 0V and no p-GaN was used. In our previous experiments with p-GaN on a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier, a threshold voltage limited to about 0.7 V and a total resistance R_{on} of 10 Ohm.mm have been achieved [10]. The gate length was 2.5 µm and we estimate this difference to account for less than 1 Ohm.mm, which confirms the interest of the present approach. At V_{gs}=+5V, the thermal effect is showing up as a slight decrease of the drain current for increasing V_{ds} (Fig.4.a). On the other hand, a very limited drain current hysteresis is noticed for V_{gs} superior to +3.5V while sweeping the gate bias upward and backward between 0V and +5V (Fig.4.b). This confirms the good quality of the interface between the p-GaN and the AlN layers.

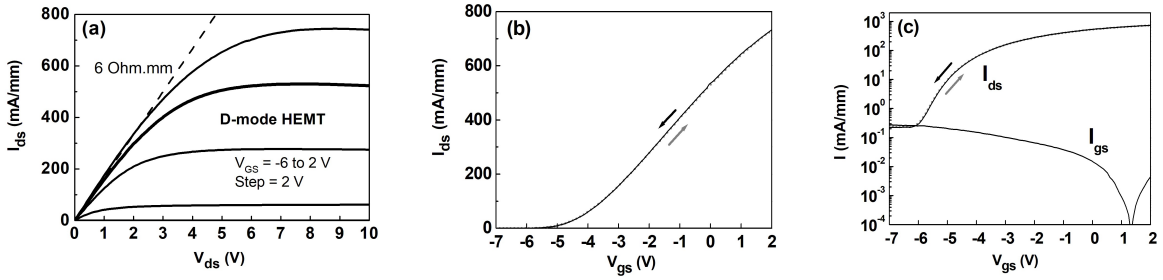

Figure 5. (a) DC output characteristics of a 1.5 µm gate D-mode transistor. (b) Hysteresis transfer characteristics at V_{ds} = 7V. Solid line shows I_{ds} for positive sweep of the gate bias; dashed line represents I_{ds} for negative sweep of gate bias. (c) Log plot of the drain current I_{ds} and the gate current I_{gs} recorded in the same conditions.

The DC output and transfer characteristics of a D-mode transistor are shown in Figure 5. The pinch-off voltage V_{th} is -5.6 V and the total resistance R_{on} extracted from the slope of the linear region of I_{ds}-V_{ds} curves is 6 Ohm.mm (Fig.5.a). The drain current at V_{gs}=0V is around 500 mA/mm and overpasses 700 mA/mm at V_{gs}=+2V without noticeable hysteresis (Fig.4.b). This current is almost double of the one previously achieved without AlGaN regrowth in a D-mode transistor on a 15 nm $Al_{0.26}Ga_{0.74}N$ barrier co-integrated with an E-mode device [10].

Conclusion

In the present work, the combination of selective area sublimation of the p-GaN cap layer and the regrowth of AlGaN have been demonstrated to fabricate an enhancement mode p-GaN/AlN/GaN HEMT device with a threshold voltage V_{gs} greater than +1.5 V and a good resistance R_{on} of 8 ohm.mm. Starting from a heterostructure with a sheet resistance of the order of 1 MOhm, the present result clearly shows the determinant positive impact of the regrowth of AlGaN in the access regions of the transistor. Furthermore, the compatibility of the regrowth with the fabrication of depletion mode transistors in large areas covered with AlGaN is demonstrated with a transistor delivering drain current density above 500 mA/mm at V_{gs} = 0 V. Both depletion mode and enhancement mode transistors are monolithically integrated using the same fabrication process. They present better performances compared to our previous developments solely based on the sublimation of p-GaN from a p-GaN/AlGaN/GaN HEMT structure; the latter are penalized by the necessary trade-off to be made between threshold voltage and access resistances. This demonstrates the interest of the proposed approach for the fabrication of enhancement mode GaN transistors as well as their co-integration with depletion mode ones.

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