D-Band CMOS Power Amplifiers: Challenges, State-of-the-Art, Technological Limitations and Trends

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***Abstract*— To achieve ultra-high-speed wireless communications, millimeter-wave bands have emerged as bands of interest for these new applications. However, a technological breakthrough linked to power amplifiers has appeared. Indeed, working near the maximum oscillation frequency of the transistor leads to low intrinsic gain and poor efficiency for these devices. This paper presents an overview of sub-terahertz CMOS power amplifiers with a focus on gain enhancement techniques. The paper will also feature state-of-the-art D-Band CMOS power amplifier architectures. The goal is to present how the gain enhancement techniques are used in a complete architecture. Based on the three techniques and the state-of-the-art presented in the paper, a focus on three architectures is proposed. The aim is to highlight the benefits of each method in the design. The final part summarizes the paper and opens up future perspectives and trends identified through the paper.**

***Index Terms*— D-Band; CMOS Power Amplifier (PA); sub-terahertz (sub-THz); unilateral power gain (U); gain-boosting**

I. INTRODUCTION

The upper millimeter-wave spectrum [150GHz - 300GHz] and terahertz [0.3THz - 3THz] bands have recently emerged as promising frequencies for various applications, including high-speed communications, high-resolution sensing, and spectroscopy. Focusing on high-speed communications, the D-Band [110GHz - 170GHz] is particularly suitable for such applications thanks to its high carrier frequency and wide available spectrum. Fig. 1, extracted from [1], shows the evolution of the data rate over the years. The data rate increase through the years needs higher bandwidth and spectrum to achieve the required performances. This highlights the interest in D-Band communication in continuous improvement of wireless data rate.

To enable the implementation of such systems in large volumes, CMOS technology has been used in numerous works [2-5] due to the low cost of manufacture. However, due to the operating frequency being close to the maximum oscillation frequency (f_{max}) of the transistor, there is a low power gain available from each transistor. The consequences are low output power for the transistor and high power consumption, leading to low power efficiency of the overall architecture. To tackle the mentioned problem, most of the work is focused on increasing the gain of each transistor when it operates near f_{max}. Based on S. Mason's work [6], the unilateral gain (U) is defined for all 2-port networks and so, this metric can be used for transistors used in common source configuration. Multiple techniques are used to enhance the gain of transistors [7-11], such as gain-boosting networks or neutralization. The gain-boosting method aims to reach the

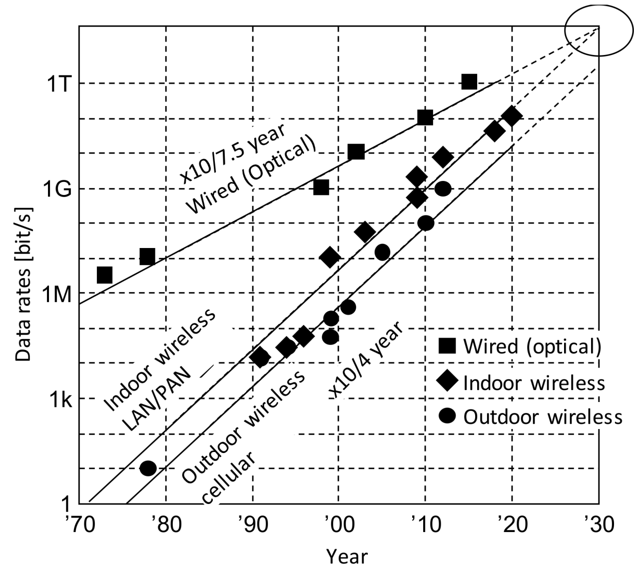

Fig. 1: Evolution of Data Rate of Wired Communication and Wireless Communication Through the Year.

maximum power gain of the 2-port active network (2-PAN) based on an optimized linear, lossless, and reciprocal (LLR) network. Neutralization is based on compensating the C_{gd} capacitance of the transistor, which becomes a limiting factor at high frequencies and causes a drop in gain. However, the implementation of these methods requires calculating the sizes of the transistors to achieve targeted performances, determining the convenient network and taking into account the losses brought by interconnections and passive components. But the higher the frequency, the higher the losses in passive components due to the electromagnetic (EM) effect, coupling, and resistivity of metal level. Moreover, targeting high gain, output power, and efficiency requires a more complex architecture and meticulous work to optimize the passive components for matching, combining, and dividing the power.

The paper is organized as follows. Section II overviews the transistor's behavior at sub-THz frequencies and the basic gain definitions for a 2-port active network. It describes the methodology to design single-peak gain-boosting and dual-peak gain-boosting. It also highlights gain enhancement based on the neutralization technique. Section III presents a State-of-the-Art of D-Band PAs with different technologies. Based on the State-of-the-Art, D-Band PA architectures are presented using the proposed gain-boosting method. Finally, the paper is concluded in Section V.

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II. Gain enhancement method at sub-THz frequencies

A. Definition of gain parameters U, G_{ma}, and G_{max}

A transistor can be seen as a 2-port active network (2-PAN) characterized by its Y-matrix as shown in Fig. 2.

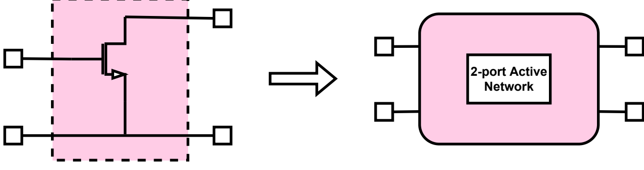


Fig. 2: Block Scheme of a 2-Port Active Network.

Mason's gain or unilateral power gain (U) can be written in terms of Y parameters based on the following equation:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(Re(Y_{11}) * Re(Y_{22}) - Re(Y_{21}) * Re(Y_{12}))} \quad (1)$$

Based on [12], the formula proposed to calculate U can be written in the same way using Z and S parameters. This gain can be seen as a Figure of Merit (FoM) for the transistor to compare their performances and moreover evaluate the f_{max}.

The f_{max} can be evaluated as the frequency where U(f_{max}) is equal to 1 or 0dB. Two other gains can be derived from U. The first one is the maximum available gain G_{ma} defined, using the stability factor K, as:

$$G_{ma} = \frac{|A|}{K + \sqrt{K^2 - 1}} \quad \text{with} \quad A = \frac{Y_{21}}{Y_{12}} \quad (2)$$

The last gain defined here is the maximum achievable gain G_{max} considered as the maximum power gain that can be reached from a transistor. This gain is defined using Mason's gain as follows:

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)} \quad (3)$$

These 3 gains can be plotted simultaneously, resulting in the curve in Fig. 3. The transistor's size used is $W = 20\mu m$ and $L = 30nm$ in the 28nm FDSOI process from STMicroelectronics.

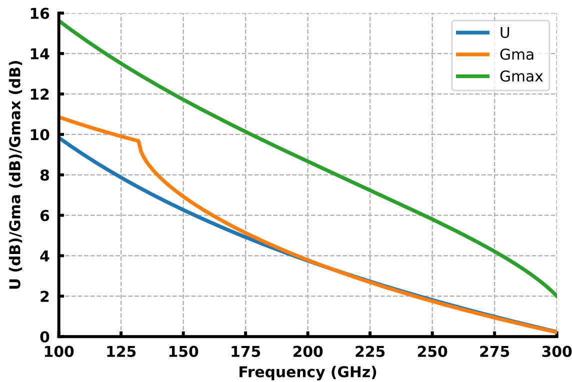


Fig. 3: U, G_{ma}, and G_{max} Plotted for a Transistor With $W = 20\mu m$ and $L = 30nm$.

The G_{max} is the maximum power gain that can be pulled out from a single transistor. The purpose of the enhancement gain technique is to reach this gain based on the enhancement of G_{ma} at a specified frequency.

The next three parts will focus on the enhancement gain technique mentioned in Section I.

B. Single-peak gain-boosting method

Based on the 2-PAN described in the previous part, a gain-boosting network can be added between the input and the output of the 2-PAN to increase the G_{ma} and assure stability. Fig. 4 highlights the block schematic of the method.

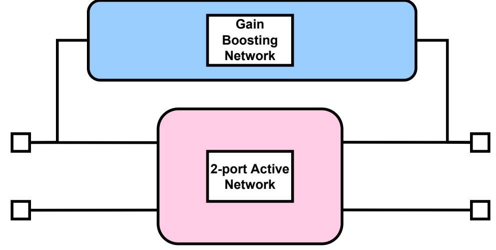


Fig. 4: Block Scheme of a 2-Port Active Network With a Gain-Boosting Network.

The purpose of the single-peak gain-boosting method is to determine a value of the inductance L_{boost} in order to increase G_{ma} at the desired frequency. The schematic of the transistor with a gain-boosting network is shown in Fig. 5.

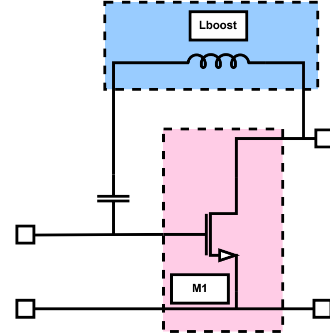


Fig. 5: Schematic of a Transistor With a Single-Peak Gain-Boosting Network.

A capacitance is added for decoupling gate and drain supplies. Design methodology are presented in [7], [12] and [13]. Two ways can be used to determine the optimum L_{boost} at a targeted frequency. To illustrate the methodology, we took an example at a specified frequency of 152GHz is used. Considering the same transistor (W = 20μm) and the same process (28nm FDSOI), U, G_{ma}, and G_{max} are plotted in Fig. 6.

As mentioned previously, the purpose of this method is to enhance the G_{ma} to get closer to G_{max} at one frequency. Without gain enhancement, the G_{ma} is equal to 6.8dB, and the increase at $f_c = 152$GHz is 3.7dB reaching 10.5dB with the gain-boosting network. It can be noticed that the gain-boosting network does not impact the unilateral gain U and the maximum achievable gain G_{max} confirming the theory developed in [6]. However, the increase of G_{ma} with this kind of network induces a low bandwidth. The resonance made with the single-peak gain-boosting network is targeted

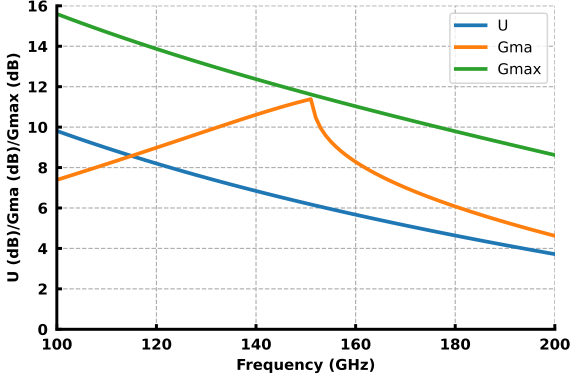


Fig. 6: U, G_{ma}, and G_{max} Plotted for a Transistor with $W = 20\mu m$ and $L = 30nm$ with Single-Peak Gain-Boosting Network.

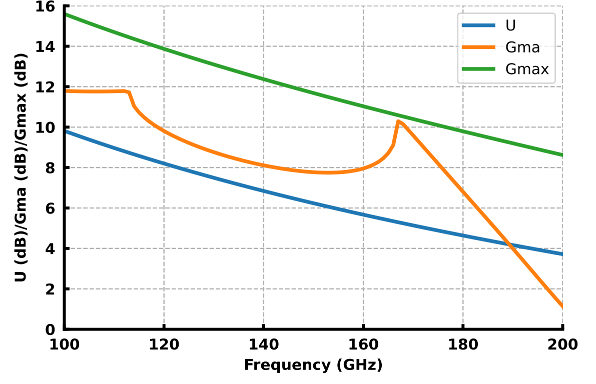


Fig. 8: U, G_{ma}, and G_{max} Plotted for a Transistor with $W = 20\mu m$ And $L = 30nm$ Using Dual-Peak Gain-Boosting Network.

at a single frequency and does not allow high bandwidth architecture. Achieving high bandwidth requires another gain-boosting network based on 2 resonances. These networks are presented in the next part.

C. Dual-peak gain-boosting method

The previous gain-boosting network is calculated at a single targeted frequency and intrinsically leads to a small bandwidth. In order to increase the bandwidth of the PA architecture, a dual-peak gain-boosting network is proposed. This network, inspired by [9], is not targeted at a single frequency, but two located at the band edges. Based on a T-shaped network with two capacitances and an inductor, the network is presented in Fig. 7

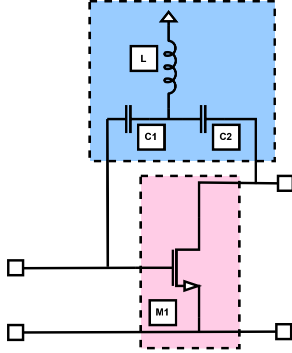


Fig. 7: Schematic of a Transistor with a Dual-Peak Gain-Boosting Network.

The two couples L/C_1 and L/C_2 are resonating at the two targeted frequencies. Based on the 28nm FDSOI process from STMicroelectronics and a transistor's size of $W = 20\mu m$, Fig. 8 presents U, G_{ma}, and G_{max} for the new gain-boosting method.

An enhancement of 1.1dB on G_{ma} is seen at $f_c = 152$GHz, this enhancement is located around the band of interest [115-165 GHz]. Two advantages can be found for this structure from the previous one: the first one is the wideband behavior of the proposed stages and the second one, there are multiple possibilities to achieve the wanted G_{ma} behavior. However, the obtained G_{ma} is lower than the single-peak network dropping from 10.5dB to 7.7dB at the same frequency, but this network leads to a higher bandwidth on the G_{ma} going from 21GHz to 44GHz considering the 3dB around 152GHz.

D. Neutralization method

The last method addressed here is the most commonly used in D-Band architecture: the neutralization method. The purpose is to neutralize the intrinsic capacitance C_{gd} of the MOS transistor by adding a capacitance with the same value as represented in Fig. 9.

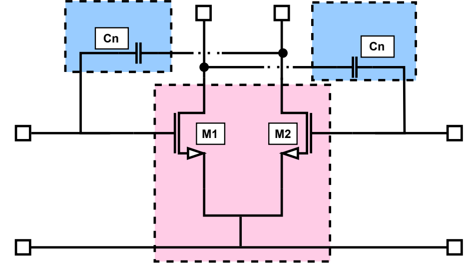


Fig. 9: Schematic of a Differential Pair Using Neutralization Capacitance.

For lower-frequency applications, these two neutralization capacitances (C_n) are used to stabilize the differential pair. However, it can also help to increase the G_{ma} of the stage [14-16]. Fig. 10 shows the increase of G_{ma} at a fixed frequency, depending on the value of C_n. It also highlights the value of k to determine if the stage is stable or not.

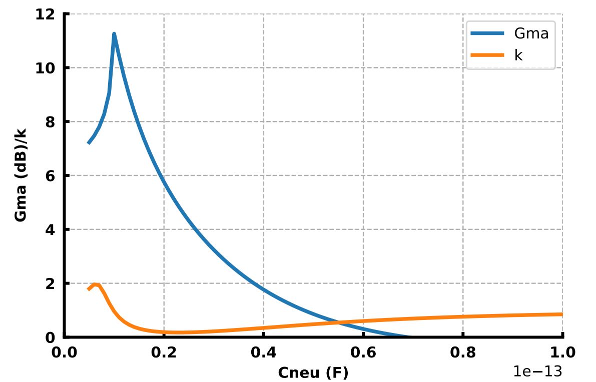


Fig. 10: k, G_{ma} and G_{max} Plotted For a Differential Pair With $W = 20\mu m$ and $L = 30nm$ Depending on the Neutralization Capacitance Value.

The stability factor k and G_{ma} are dependent on C_n but the maximum of each is not achieved for the same value. Based on this, a compromise needs to be found to ensure a higher gain and stability. Considering the proposed case, a capacitance of 8fF is chosen to increase the G_{ma} of the differential pair and ensure stability. U, G_{ma}, and G_{max} are plotted in Fig. 11 to highlight the improvement.

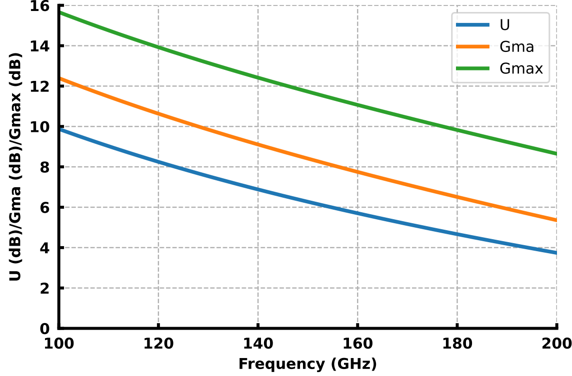


Fig. 11: U, G_{ma}, And G_{max} Plotted for a Differential Pair with $W = 20\mu m$ And $L = 30nm$ Using Neutralization Capacitances.

Without gain enhancement, the G_{ma} is equal to 6.8dB, and the increase at $f_c = 152$GHz is 1.5dB reaching 8.3dB with the neutralization method.

Three methods are presented here to improve the intrinsic gain of a single transistor or a differential pair. The achieved performances of each method are summarized in Table 1.

Table I.: Summary of Achieve G_{ma} with Gain Boosting Networks.

	G_{ma} at f_c = 152GHz	3dB BW @ f_c
No gain-boosting network	6.8dB	35GHz
Single-peak gain-boosting	10.5dB	46GHz
Dual-peak gain-boosting	7.7dB	72GHz
Neutralization	8.5dB	49GHz

Even though U and G_{ma} are characterized by small-signal parameters, their values are close to the expected power gain value in large signal simulations. Considering D-Band power amplifier, these metrics are the first approach to evaluate the total gain available for an architecture.

The next Section proposed to overview the performances of D-Band PA through the literature and described architectures of D-Band PA using the proposed gain enhancement methods, which have performances at the forefront of State-of-the-Art.

III. State-of-the-Art D-Band Power Amplifiers

To highlight the expected performances of D-Band PA, a State-of-the-Art is done targeting three main performances: output Gain, saturation power (P_{sat}) and Power-Added Efficiency (PAE). Different technologies are taken into account, extracted from [2-5] and [7-27].

Fig. 12 depicts the gain achieved by the various studies collected. In the D-band, the gain varies between 10 dB and 25 dB, with a slight decrease when the proposed works are in the higher part of the band. It is also important

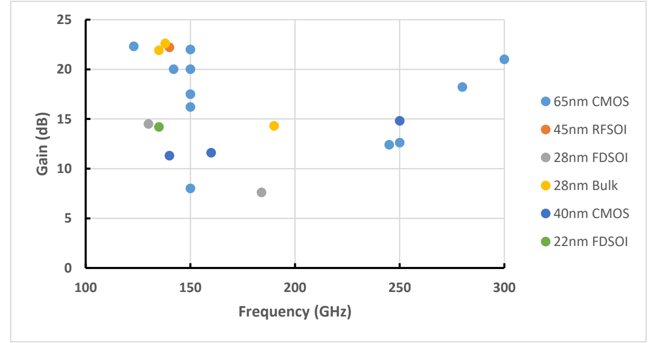


Fig. 12: Gain Achieved for Power Amplifier in Different Technologies.

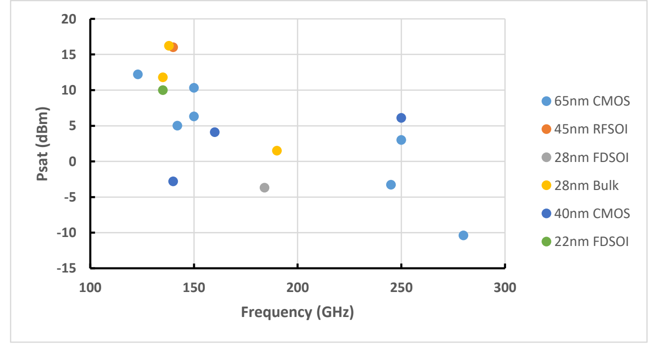


Fig. 13: Output Power Achieved for Power Amplifier in Different Technologies.

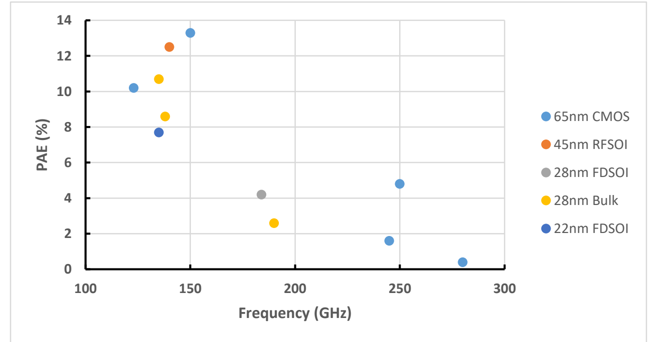


Fig. 14: PAE Achieve for Power Amplifier in Different Technologies.

not to overlook studies conducted at over 200 GHz, which may exhibit significant gain values. However, these studies still struggle to attain adequate output power and efficiency. About the P_{sat}, Fig. 13 illustrates the results obtained for various architectures. A clear trend line is evident, indicating that P_{sat} decreases as the operating frequency increases. This phenomenon is thus correlated with the need to optimize f_{max} and, consequently, reduce the margin for current density passing through the transistor. This current density limitation is inherently linked to the maximum output power of the PA. The same observation can be made for the PAE (Power-Added Efficiency), presented in Fig. 14, with a decreasing trend line as a function of frequency. For D-band works, it does not exceed 15% in CMOS technology. These values can be explained by the transistor's low intrinsic gain and the need for high biasing of the stages used.

The next section will present architectures that are on the cutting edge of State-of-the-Art. The purpose is to demonstrate the usefulness of each method presented in Section II.

IV. Architecture of D-Band Power Amplifiers

A. D-Band Power Amplifier using single-peak gain boosting

Based on the work in [27] and to illustrate the single-peak gain-boosting method, a 4-stage D-Band PA is presented slightly above the D band. It highlights a G_{ma} increase of 3.7dB for each stage before implementing it in the complete architecture. The first step to achieve this type of architecture is to evaluate the correct network to increase the G_{ma}. Fig. 15 shows the evolution of the intrinsic gain of the transistor depending on the value of inductors around the transistor.

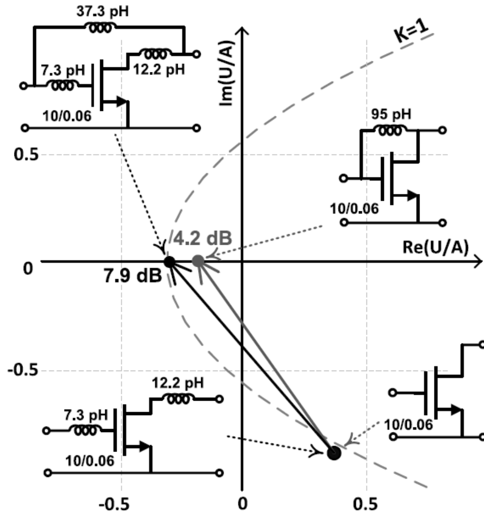
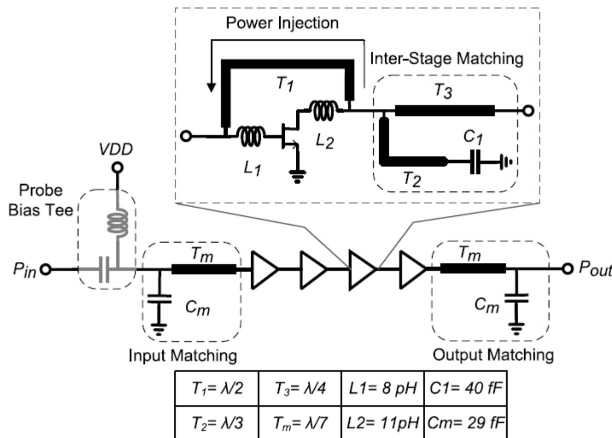


Fig. 15: Evolution of G_{ma} for Different Inductors Values [27].

The dual purpose of the network is to increase the gain and also ensure the stability of the transistor. Once the network is evaluated and implemented, a 4-stage single architecture is proposed using input and output stub matching as shown in Fig. 16.

The PA is manufactured in 65nm CMOS. Fig. 17 shows the setup used for measurements.



$T_1 = \lambda/2$	$T_3 = \lambda/4$	L1= 8 pH	C1= 40 fF
$T_2 = \lambda/3$	$T_m = \lambda/7$	L2= 11pH	Cm= 29 fF

Fig. 16: Schematic of the 4-Stage Single Peak Gain-Boosting PA [27].

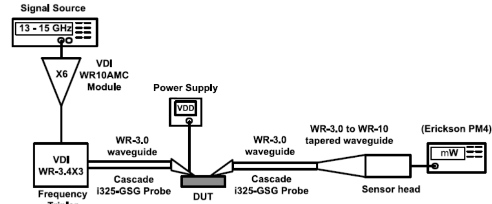


Fig. 17: Test Setup for Large-Signal Measurements [27].

The obtained S-parameters are presented in Fig. 18. The amplifier has a maximum measured small-signal gain of 9.2 dB at 257 GHz and the input and output reflection coefficients of -5.5 and -8.5 dB, respectively. The 3dB bandwidth achieved by the architecture is 12.2GHz.

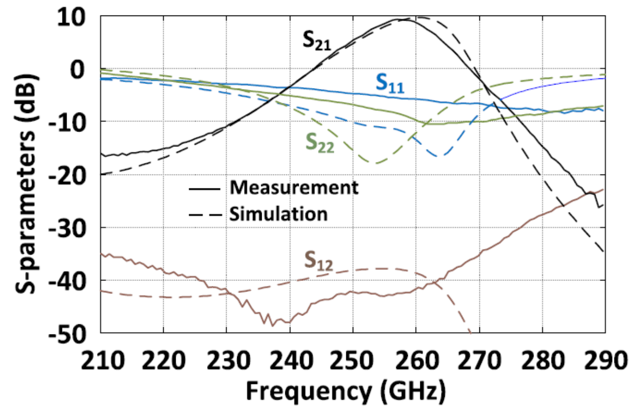


Fig. 18: Measured and Simulated S-Parameters for the 4-Stage Power Amplifier [27].

As shown in Fig. 19, at 255 GHz, the maximum PAE is 1.35% and the maximum P_{sat} is -3.9 dBm with V_{DD} = 1 V. The amplifier consumes 27.6 mW at VDD = 1 V.

The purpose is to show the feasibility of the method and implement it in a complete PA architecture. Despite the low bandwidth displayed, the architecture proposes small and large signal measurements that validate the functionality of the circuit.

Another interest of this single-peak embedding is the possibility of using them in addition to other gain enhancement techniques [30]. In this work, the proposed architecture is a

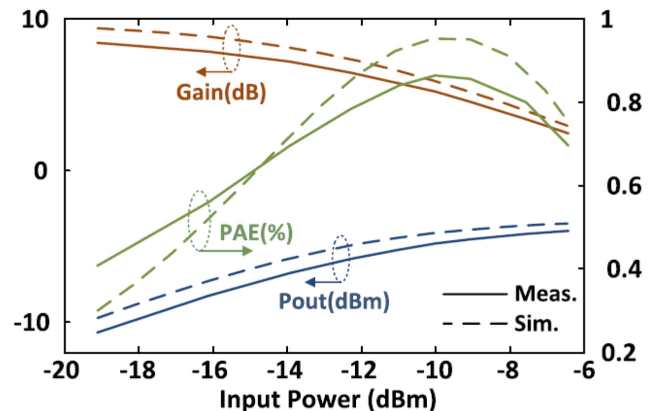


Fig. 19: Power Added Efficiency, Output Power, and Large-Signal Gain of the Amplifier for V_{DD} = 1V [27].

4-stage PA working at 160GHz. The block view of the PA is presented in Fig. 20.

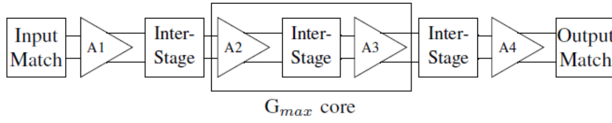


Fig. 20: Block view of the PA [32].

All stages are based on neutralized differential pairs; however, the distinctive feature of this architecture lies in stages 2 and 3. To enhance the G_{ma} of this section, a single-peak gain-boosting network is employed around these two stages. The resulting layout is presented in Fig. 22.

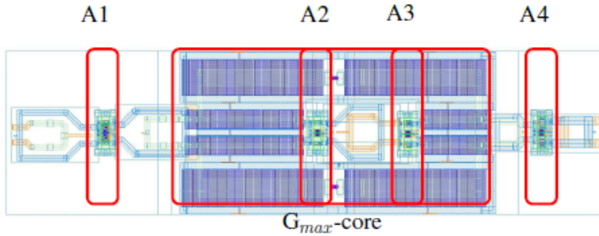


Fig. 21: Layout view of the PA [32].

The four stages are visible, with special attention given to the A2-A3 couple, where the gain-boosting network is incorporated to enhance the power gain. This implementation results in a 3.1dB enhancement at 160GHz, in addition to the initial improvement achieved by the neutralization capacitance. As mentioned by the author, the network was designed to ensure a stability factor equal to 1. This low k-factor can lead to instability in measurements and is sensitive to process variations. The paper proposes Post-Layout Simulations (PLS) at 160GHz, considering large signal parameters of the PA: Gain, P_{sat}, and PAE. The results obtained are shown in Fig. 22. The PA achieves an OP_{1dB} of 5 dBm and P_{sat} of 11 dBm with a gain of 32dB. The peak PAE is 9.8%. The PA consumes power of 112 mW from a 1.1 V supply.

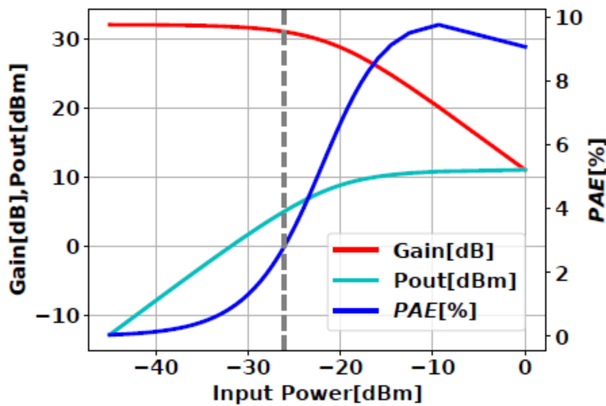


Fig. 22: Large signal gain, Power Added Efficiency and output power of the PA [32].

B. D-Band Power Amplifier using dual-peak gain boost-ing

Another interesting work done in [9] gives an example of a dual-peak gain boosting network to overcome the performance limitations of CMOS technology at frequencies exceeding 100 GHz. The concept of a T-embedding network has been explored to enhance the G_{ma}. In this study, an innovative Gmax-core incorporating a T-shaped gain-boosting network that provides two G_{ma} peaks is analyzed and demonstrated in the D-band using a 28nm FD-SOI CMOS process. The proposed methodology for the multi-stage design is the following: each stage has its own G_{ma} behavior, enabling achieving a wider bandwidth at the end. Fig. 23 shows the modification of G_{ma} behavior, starting from a single transistor to a transistor with the proposed T-embedding network.

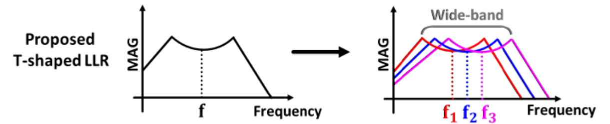


Fig. 23: Strategy of Broadband Amplifier Design [9].

This type of network provides another useful feature: the input and output impedances can be adjusted based on the T-network combinations. Indeed, a good choice of network can provide a lower frequency dependency of the input and output impedance of the stage. It results in a wideband matching thanks to impedance transformers commonly used in the literature.

Based on these considerations, the schematic view of the PA is presented in Fig. 24 and the layout view in Fig. 25.

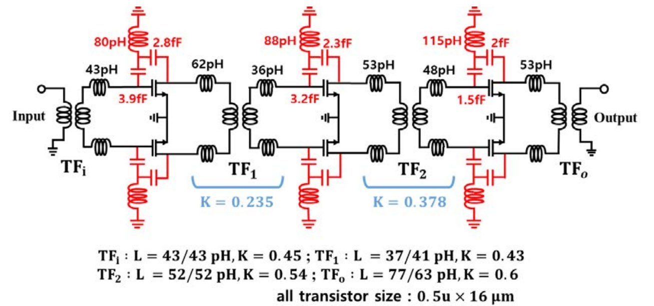


Fig. 24: Schematic of the Proposed D-Band Amplifier With T-Shaped Embedding Network [9].

The proposed D-Band PA is a 3-stage broadband amplifier using the method presented above. The proposed T-shaped network is implemented in 28nm FD-SOI CMOS. Small signal S-parameters were measured using a WNA and a WR-6.5 frequency extender. The obtained results are presented in Fig. 26.

The amplifiers exhibit a power gain and 3dB bandwidth of 14.5 dB and 26 GHz [117GHz - 143 GHz], respectively, with a power dissipation of 21.6 mW. Despite the great performances achieved by the PA in small signal parameters, no information is available for large signal behavior and the P_{sat}, compression point, and PAE can not be evaluated.

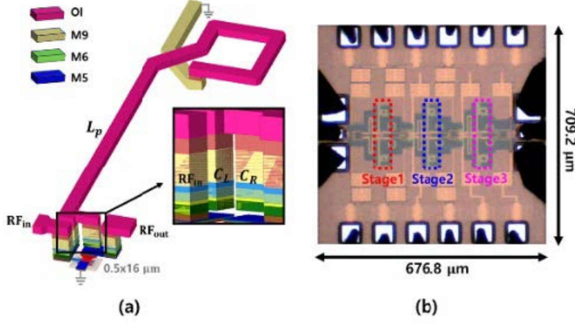


Fig. 25: (a) Core Layout (b) Chip Microphotograph [9].

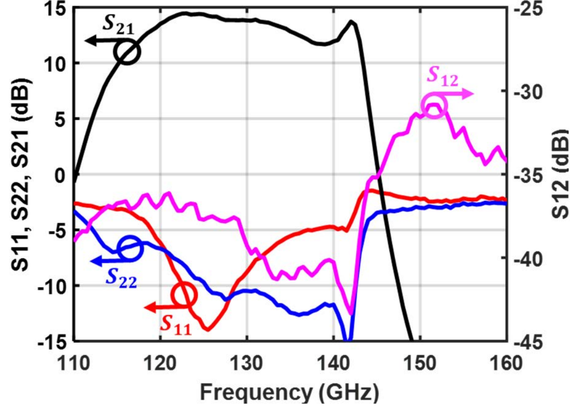


Fig. 26: Measured S-Parameters [9].

To conclude on single and dual-peak gain-boosting networks, the trend indicates that these types of networks can be used for D-Band architecture. However, most architectures utilizing these networks exclusively apply them across all stages. As mentioned earlier, considering the active part with gain-boosting modifies the k-factor, bringing it closer to 1. This low stability factor results in lower power levels due to the circuit's sensitivity when a high power level is applied. The major risk is an oscillating power amplifier (PA). Alternatively, gain-boosting can also be employed in addition to neutralized stages, leading to high-gain stages. It is important to highlight that this is primarily used for gain stages. If power levels are too high, the risks are similar to those of other architectures.

C. D-Band Power Amplifier using neutralization capacitances

This part focuses on a 4-stage D-Band PA achieving the highest performances in Gain, P_{sat} and PAE [18]. Based on neutralization capacitances (C_n), the PA first proposes a 4-stage differential cell which is combined in a 4-way PA to achieve the obtained performances. This work highlights the two points targeted in this paper. The first one is the gain enhancement using the neutralization method. This method is commonly used in numerous works in D-Band, but also at lower frequency.

Based on the method presented in Section II, the first goal is to evaluate the optimal value of C_n. Fig. 27 shows the behavior of G_{ma} and k depending on the value of C_n.

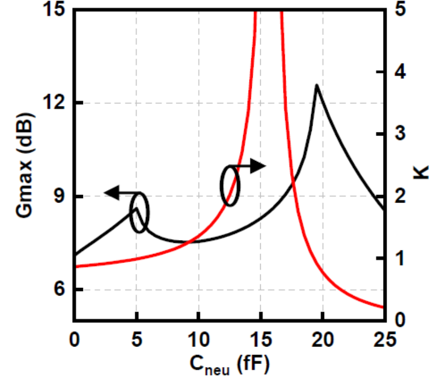


Fig. 27: k and G_{ma} Depending on C_n [18].

The value of C_n needs to be chosen to increase G_{ma} and ensure the stability of the stage. In this work, due to the increase of transistor's sizes through the stage, the capacitances are chosen equal to 7fF for the two gain stages, 9fF for the driver and 10fF for the power stage. The schematic of the differential PA single cell is presented in Fig. 28.

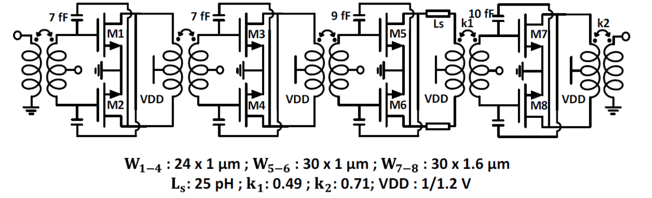


Fig. 28: Schematic of the Differential PA Single Cell [18].

As for the previous work and due to the low intrinsic gain of each stage, the architecture needs multiple stages to achieve enough power gain. This leads to the design of passive components such as impedance transformers and power combiners. The first one helps to achieve impedance matching between the stages and the second one helps to achieve higher P_{sat}. In both cases, losses in these components must be minimized to not compromise the work performed on the active part and also try to keep power efficiency as high as possible. This point will be developed from now on. Based on the previous differential PA cell, a 4-way power combination is proposed to achieve a P_{sat} of 17.5dBm at 140GHz. To do so, the schematic of the complete architecture is presented in Fig. 29 and the fabricated PA, in 45nm RFSOI, is shown in Fig. 30.

Three cases need to be distinguished. Input and output baluns are used for impedance matching and single-to-differential conversion. Interstage transformers are used for interstage matching. Power combiners are used to combine the four output ways to increase the maximum output power.

Starting with input and output baluns, the target is to have highly coupled baluns to achieve low loss and power matching. High coupling coefficients are achieved using symmetrical baluns. However, the bandwidth of the baluns is intrinsically linked to the coupling coefficient between the two inductors. A high coupling coefficient results in narrowband matching, but methods are proposed to increase the bandwidth of such baluns [28]. About the interstage transformer, the preferred topology is asymmetric transformer. It enables

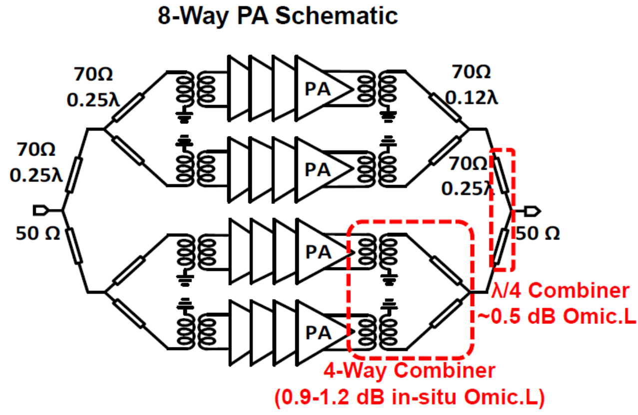


Fig. 29: Schematic of the Complete 4-Way PA [18].

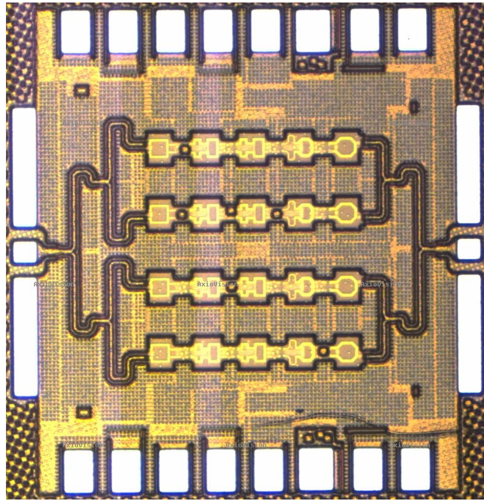


Fig. 30: Layout of the Complete 4-Way PA [18].

both impedances simultaneously without adding other components. Fig. 31 shows an example of an asymmetric transformer used in the design.

However, it requires being careful of the coupling coefficient and quality factor of the inductors used for the design. Losses of the transformers are linked to these two parameters. Thick levels of metals are to be preferred for this design to reduce the skin effect, increase the quality factor of the inductors, and manage properly the coupling coefficient.

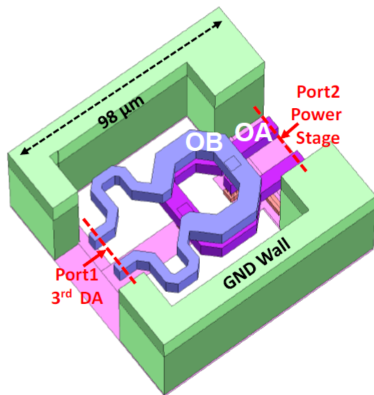


Fig. 31: Interstage Matching Asymmetrical Transformer [18].

The last part highlights the design of power combiners used in D-Band architectures. Most of the combiners are 0° combiners based on Wilkinson topologies. Working at high frequencies (above 100GHz) enables the integration of such combiners based on $\frac{\lambda}{4}$ lines which became small enough to be integrated. The main default of these combiners is the non-possibility of matching. However, [28] and [29] proposed solutions to co-design power combinations and matching networks. An example of these combiners is proposed in Fig. 32.

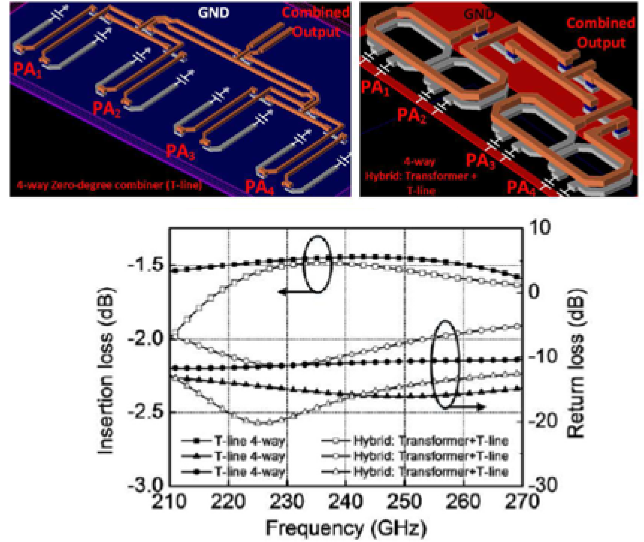


Fig. 32: Zero-Degree Combiner with Matching Network [28].

This structure combines 4 differential ways with insertion losses of 1.4dB which is acceptable for D-band design considering the number of combinations.

Based on these considerations, the PA proposed in [18] achieves the performances in small-signal parameters shown in Fig. 33 and continuous wave (CW) measurements are shown in Fig. 34.

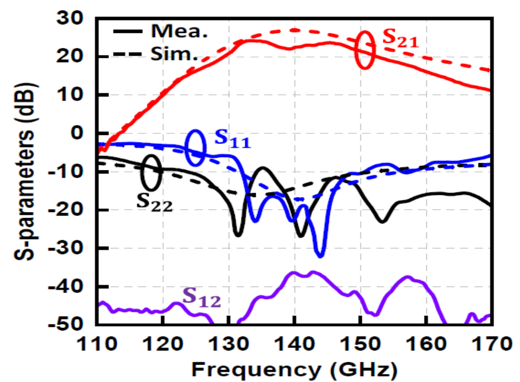


Fig. 33: S-Parameters of the 4-Way Differential PA [18].

The PA achieves a 3dB bandwidth of 19GHz from 131GHz to 150GHz with a gain ripple of 1dB. S_{11} and S_{22} are below -10dB in-band.

Considering the CW, gain and PAE are plotted according to the input power P_{in}. The characterization is made at f = 140GHz.

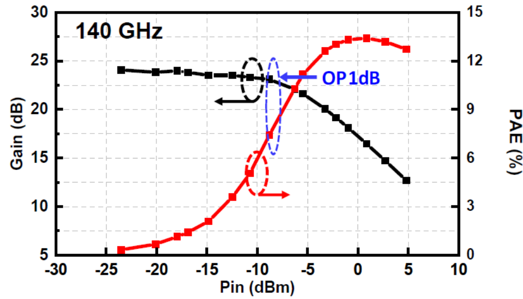


Fig. 34: Continuous Wave Characterization of the 4-Way Differential PA at 140GHz [18].

The power gain achieved is 24dB at 140GHz with P_{sat} of 17.5dBm and maximum PAE of 13.4%. The proposed D-Band PA achieves high output power, linearity and efficiency using neutralization enhancement gain technique as well as low loss 8-way power combining. This work highlights the best FoM seen in State-of-the-Art.

As a conclusion to this Section, all the performances achieved by the presented architectures are summarized in Table II. For comparison, a Figure of Merit (FoM) is introduced. The architecture employing a neutralization method emerges as the optimal solution for applications requiring higher power, while the boosting method proves particularly well-suited for gain stages operating at lower power. This dual approach provides optimal flexibility to meet diverse performance requirements.

V. Assessment of State-of-the-Art and Prospective

This paper presents an overview of D-Band PAs with the challenges and technological limitations appearing through the design. Multiple complete PA architectures are presented after the characterization of various enhancement gain techniques such as single and dual-peak gain boosting or neutralization capacitances by simulations. Trends followed by State-of-the-Art can then be highlighted. Considering the gain-boosting method, most of the work do not highlight large-signal measurements and limits the study to S-parameters. However, it brings multiple possibilities for the designer like bandwidth increase and input and output impedance control of the power cell. Best-in-class PA processed in 45nm RF-SOI uses neutralization capacitances. It highlights the best performances around 140GHz, with the idea to simplify the active part with a well-known method and focus the major part of the work on passive components.

Considering the various points addressed in this paper, it is clear that the intrinsic gain of the transistor alone is not sufficient. Gain-boosting networks must be added to complete architectures with efficiency exceeding 10%. In the context of future work, it is essential to validate the operation and understanding of these networks, particularly those relying on conditions close to transistor oscillation. The designer's task will be to ensure the model's validity and proper use of the networks, especially during high-output power tests. Finally, the role of passive components should not be underestimated. Given the state of the art, the combination of multiple paths appears to be the best approach to obtaining high-performance architectures. However, this combination must be carefully managed to minimize losses and avoid further degradation of the limited available gain from active stages.

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Table II.: State-of-the-Art for D-Band architecture.

	[27]	[32]	[9]	[18]
Process	65nm CMOS	28nm FDSOI	28nm FDSOI	45nm RFSOI
f_{max} [GHz]	345	291	291	270
Operation frequency [GHz]	257	160	130	140
Gain [dB]	9.2	32	14.5	22.2
P_{sat} [dBm]	-3.9	11	N.A*	16
3dB BW [GHz]	12.2	7	26	21
DC power [mW]	27.6	112	21.6	305
peak PAE [%]	0.8	9.8	N.A*	13.4
Area [mm^2]	0.14	0.052	0.1	0.43
FoM*	26	69.9	N.A*	75.4

FoM* = Gain[dB]+Psat[dBm]+20*log(3dB BW[GHz])+10*log(Peak PAE[%])
N.A* = Non-available

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