N-Path Mixer with Wide Rejection Including the 7 th Harmonic for Low Power Multi-standard Receivers

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***Abstract*— This paper proposes an N-Path mixer rejecting a wide bandwidth 1:8, i.e. including the 7th harmonic, while keeping a low complexity, particularly suitable for low power multistandard receivers. The main principle is based on an accurate choice of the switch control signals and of the gains of the amplifiers stage. The circuit has been manufactured in 28nm FDSOI technology. Measurements prove the theory with an harmonic rejection higher than 45 dB for the 3rd, 5th, and 7th harmonics, an in-band IIP3 of -3.5 dBm, for a power consumption of 22 mW.**

Keywords—N-path mixer, software defined radio, multistandard, harmonic rejection, wideband low noise amplifier,

I. INTRODUCTION

During the two last decades, the variety of RF applications and the number of RF standards highly increased leading to a huge number of connected devices [1]. This has resulted in strong advances in the domains of RF hardware design and modern communication systems, thus opening the door towards a multitude of applications for wireless remote control: nowadays multi-standard approaches are not considered only for smartphone, but in many RF systems.

Therefore, an eco-design concern (optimization of the numbers of receivers to be manufactured, configurability of the receivers and power saving) is essential to obtain a unique RF receiver chain that is able to process different standards. There exist various approaches to design multi-standard receivers. Multiple parallel narrowband receivers have been first explored. Such solution is quite simple and robust but suffers from low integration and high power consumption [2]. On the opposite way, receivers based on wide band RF front-end and reconfigurable digital blocks solve these two issues at the expense of the performances. In such approach, the poor frequency selectivity of the RF front-end reduces the tolerance to blocker, which highly impacts the linearity requirements. To alleviate the constraints on linearity, the best way would be to use a narrowband receiver fully tunable over a wide bandwidth. In this context, N-path mixers (NPM) are very attractive as they achieve good performances, are frequency tunable and frequency selective in the meantime [3]. However, the design and the performances of tunable RF circuits such as passive filters and LNAs remain an issue since they are totally dependent on designing performing tunable passive components such as inductors. As an example, active inductor based LNA topologies have been explored but performances are still to be improved [4]. Then, a convenient solution to mitigate linearity constraint and selectivity rely on a mixed approach between wideband and tunable narrowband circuits such as offered by LNA-first N-Path receivers [5].

By the way, N-path receiver still suffers from a major issue, limiting the system bandwidth and thus the number of standards it can process. In fact, LO (local oscillator) sampling generates harmonics that can possibly induce undesired frequency folding into the IF band of interest. To solve this problem, a NPM with harmonic rejection properties, namely HR-NPM, allows rejecting these harmonics and thus increasing the harmonic rejection band. In a general way, HR-NPM rejects up to the $N-2$ harmonic included. The most popular LNA-first architecture is the HR-8PM [5], [6]. Such architecture uses several parallel branches as shown in Fig. 1 to synthesize an effective local oscillator signal ($EFLO$ in frequency domain and $eflo(t)$ in time domain) of the N^{th}=8th order having its first harmonic rising at $(N\text{-}1).F_{LO}$ [7]. Expending this architecture to increase the rejection band dramatically increases the complexity. As studied in [7], a HR-10PM would need four parallel branches with four differential LNAs, increasing power consumption and mismatch issues. This paper shows for the first time the measurements of a low complexity LNA-first HR-NPM offering a wide band from 1 to 8, that is to say including the 7th harmonic. The circuit is a modified version of the one presented in [7] in order to be more resilient to clock overlapping issues. This system requires a clock control signal of frequency $5f_{RF}$, thus releasing the constraints on the VCO and its power consumption, while keeping a complexity in terms of number of amplifiers identical to that of an HR-8PM. It has been designed in 28-FDSOI technology from ST-Microelectronics with the aim to cover a frequency band ranging from 150 MHz to 150*8=1200 MHz, including, for the first time to the authors' knowledge in such architecture, the 7th harmonic.

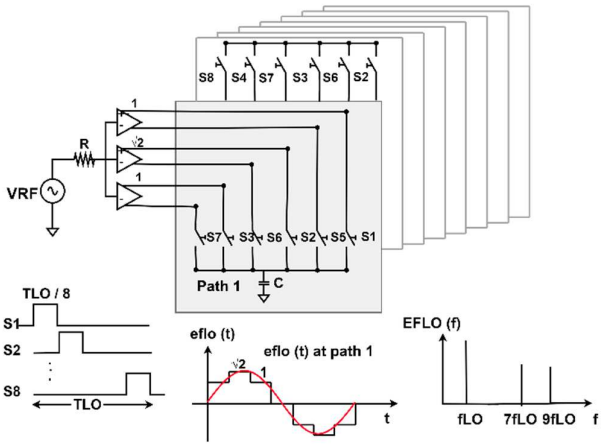

Fig. 1. Conventional LNA-first HR-8PM topology.

The theoretical principles of HR-NPMs as well as that of our original topology are presented in section II. Section III details the building blocks design. The measurements are presented for the first time and are compared with the state of the art in section IV.

II. HR-10PM$_{EQ}$ ARCHITECTURE

A. Harmonic rejection N-path mixers

HR-NPM may present two configurations either the LNA-first or the mixer-first architecture. Both architectures present interest depending on the targeted propriety. LNA-first are typically chosen for their sensitivity while mixer-first are preferred for linearity. In LNA-first architectures, gain ratios are achieved either at RF through LNAs, or at IF with baseband amplifiers, or using both [5], [6]. In [5], a harmonic rejecting N-path filter was proposed, which featured tunable-band filtering at the LNA output with high attenuation of the 3rd and 5th LO harmonics, thus improving the blocker tolerance at those frequencies. In [6], the solution was based on an analog two-stage polyphase HR concept such that this architecture reduces the harmonics mixing, rejecting the 5th LO harmonic in a way particularly robust to the mismatch.

Whatever the considered architecture (LNA- or mixer-first), the idea for harmonic rejection consists in synthesizing an $EFLO$ signal having a reduced number of harmonics when compared to the conventional square duty-cycled LO signal used in NPM. To do so, multiple parallel branches need to be connected to the capacitor path. In a conventional approach, the number of branches (H) is equal to the number of paths (N), and each branch achieves a particular gain. The gain of the h^{th} branch is equal to the value of the h^{th} sample of a sine wave of frequency F_{LO} sampled at $N.F_{LO}$ and is given by:

$$G_h = \sqrt{2}\,\sin\left(\frac{2}{N}(1+h)\right) \qquad (1)$$

As shown in Fig. 2, some sample values (i.e. gain values) are null, which reduces the number of branches to be implemented.

Since the first harmonic rises at $(N\text{-}1).F_{LO}$, the higher the harmonic rejection required, the higher the number of branches. To reject up to the 6th harmonic, 3 branches with 3 differential LNA and 48 switches are necessary. However, such harmonic rejection is not sufficient to cover a targeted bandwidth of 1:8, for which a 10th order PM (HR-10PM) is required. In a conventional structure, such harmonic rejection needs four branches to be implemented with 70 switches [3].

B. π-delayed HR-10PM

The proposed circuit is a modified version of the architecture presented in [7] and recalled in Fig. 3. It is based on a 5 capacitor paths mixer, implemented with 3 differential branches. Anyway it will be shown that the $eflo(t)$ stays the sample version of the sine wave of the HR-10PM of Fig. 2, reproduced in Fig. 3; hence it is stated that N=10. Two versions (S_n^+ and S_n^-) of 2/N=1/5 duty-cycled clock signals drive the positive and negative branches respectively. Positive branches generate $eflo^+(t)$ whereas negative branches generate $eflo^-(t)$. Both effective LO are combined in each capacitor path to form the $eflo(t)$ equivalent to the one of an HR-10PM. The negative clock signals (S_n^-) are simply the π-delayed version of the positive clock signals (S_n^+). As aforementioned, the complexity is significatively reduced when compared to the conventional HR-10PM architecture since only 3 branches and 5 capacitor paths are used. In addition, positive and negative clock signals can be derived from complementary signals, alleviating by the way the complexity.

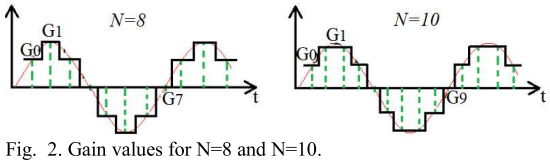

Fig. 2. Gain values for N=8 and N=10.

C. Overlapping issues

NPM are particularly sensitive to clock signals overlapping [8]. This phenomenon generates unwanted charge redistribution in the capacitors and directly affects the $EFLO$ signal. As shown in Fig. 4 where clocks overlapping is simulated by increasing the width of the S_h signals, the π–delayed HR-10PM is highly sensitive to this phenomenon. Spikes separated by a $T_{LO}/5$ time duration appear and generate strong 5th harmonics in the frequency response of the $EFLO$.

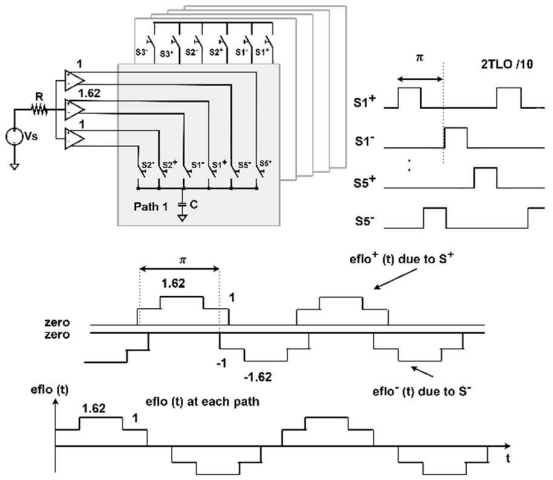

Fig. 3. Structure of the π-delayed HR-10PM [7].

To solve this issue, the clock signals (S_h) duty-cycle is reduced to 1/10 in order to avoid multiple branches to be simultaneously connected to one given capacitor path. The clock signals are arranged to produce the same $EFLO$. The modified version of the topology is presented in Fig. 5. A fully differential scheme is chosen to reduce the even harmonics.

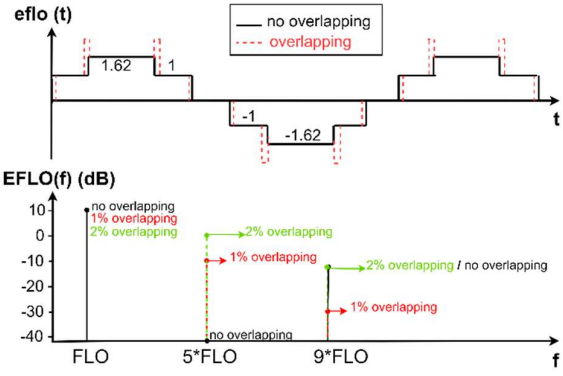

Fig. 4. Effective LO in time domain and corresponding harmonic response in frequency domain for ε =1% and ε =2% duty-cycling enlargement.

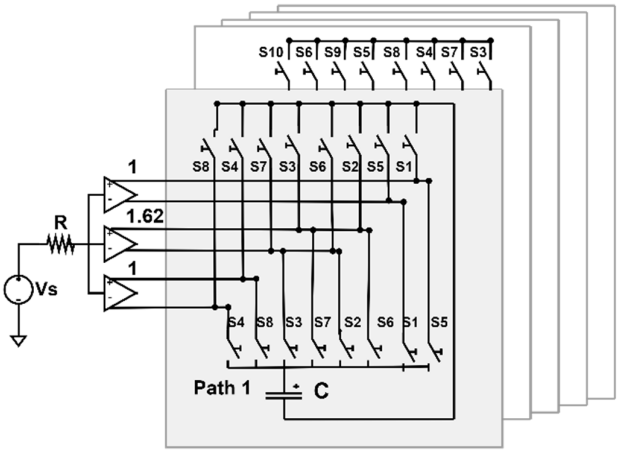

Fig. 5. Modified structure of the π-delayed HR-10PM: the HR-10PM$_{eq}$.

III. CIRCUIT DESIGN

As shown in Fig. 6, the proposed circuit is composed of a LNA block, a mixer block and a LO signal generator circuit.

A. LNA Stages

The LNA is a 2-stage amplifier. The first stage is the CGCS noise cancelling based LNA presented in Fig. 7a. It has been chosen for its wideband properties and single to differential ability in order to generate the differential signals required by the topology. The common mode at the output of the LNA dramatically impacts the harmonic rejection of the whole receiver. Since the gain of the CGCS LNA is given by:

$$G_v = G_{v,CG} - G_{v,CS} \tag{2}$$

$$= g_{m,CG}(R_{L,CG}//r_{ds,CG}) + \frac{R_{L,CG}}{r_{ds,CG}+R_{L,CG}} + g_{m,CS}(R_{L,CG}//r_{ds,CG})$$

the g_m of both stages are independently controlled through current mirror with external trimer for calibration purposes.

The second stage is composed of three differential resistive amplifiers. These amplifiers are strictly identical except for the output resistor, which is equal to 118 Ω for the two gains equaling 1 and 215 Ω for the other one achieving a gain of 1.62. In addition, the biasing current is slightly different and is externally adjusted for calibration purposes. The outputs of the amplifier are monitored through a 20-kΩ resistor to control the gain ratio and the imbalance.

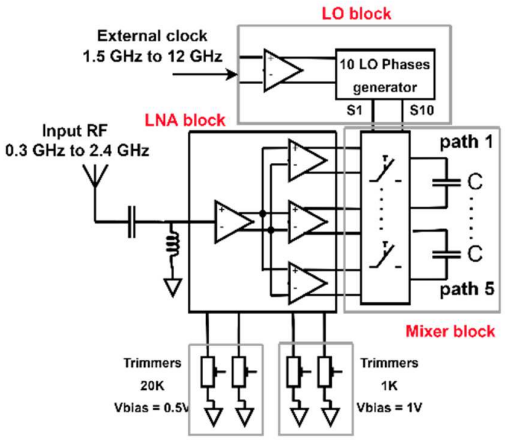

Fig. 6. System view of the HR-10PM$_{eq}$ circuit.

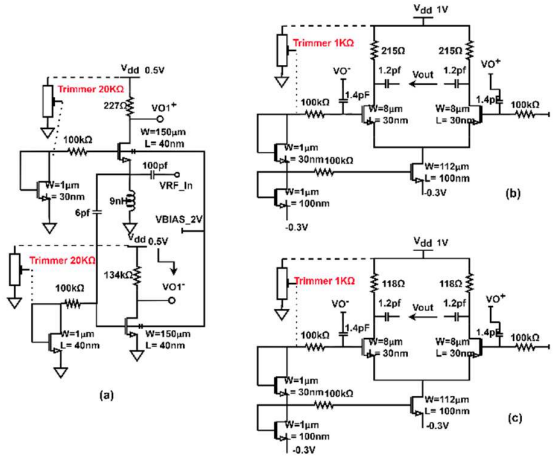

Fig. 7. (a) LNA 1st stage (b) LNA 2nd stage with relative gain 1.62 (c) LNA 2nd stage with relative gain 1. The latter is replicated twice (2 gains of 1).

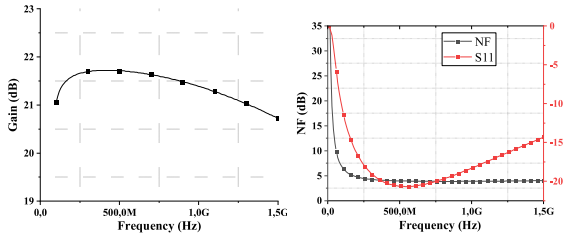

Fig. 8. Post-layout simulation of the complete LNA block (for G=1.62).

As shown in Fig. 8, where post layout simulation results are presented, the whole amplifier is designed to achieve a minimum NF of 4.8 dB around 1 GHz, with a maximum variation of 1.5dB in the targeted bandwidth, 150-1200 MHz. The S_{11} is lower than -10 dB and the maximum gain is 22 dB with a variation lower than 1 dB over the whole bandwidth.

B. Phase generator

The phase generator, presented in Fig. 9 is based on a shift register frequency divider, which is widely use in NPM system [9], [10]. As in [10], two parallel registers are driven by complementary clocks alleviating the constraint on the external clock. To generate a 1/5 duty-cycle phase, the first register is set to 1 whereas all the other registers are set to 0 at initialization. As shown in Fig. 9, 1/5 duty-cycle phases are then combined with AND gates to produce the ten, 1/10 duty-cycled, desired control signals of Fig. 5 (S_h). With this solution, the reduced constraint on clock frequency is kept while the overlapping impact on 5th harmonic disappeared.

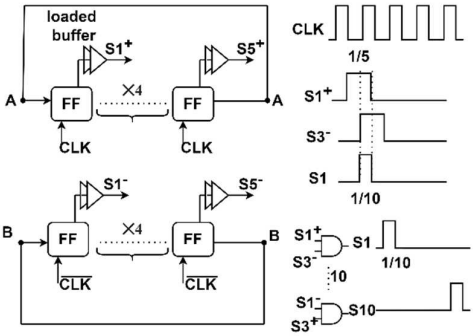

Fig. 9. Phase generator principle.

IV. MEASUREMENT RESULTS

The circuit has been implemented in 28nm FDSOI technology and packaged in a 44 QFN. As shown in Fig. 10, the circuit size is lower than 1 mm^2. The power consumption is provided in TABLE I. Mixer plus phase generator power consumption is only 2.7 mW, whereas the LNA stages consume 19.6 mW. The latter could be further optimized since LNA covers a wider bandwidth than the targeted one.

Even if the mixer outputs are DC coupled, the instrumentation amplifiers implemented on the evaluation board are AC coupled thus limiting the low frequency conversion gain. As shown in Fig. 11 where the measured S_{11} is plotted, the whole mixer is matched on the entire targeted band. Conversion gain and harmonics rejection measurements are performed for an intermediate frequency of 5 MHz. The measured conversion gain is 13 dB at 150 MHz and remains quite constant over the bandwidth ($Gc_{@1.2\ GHz}$ = 11 dB), and the measured in-band IIP3 is -3.5 dBm (Fig. 12).

A rejection level greater than 45 dB is obtained for the 3 odd harmonics (3rd, 5th and 7th). As presented in Table II that compares similar works, this is the first time a rejection of the 7th harmonic is reported. The conversion gain is lower than other work since the presented mixer do not embed baseband TIA or amplifiers. The measured NF of the whole on board receiver with external baseband amplifiers is 13 dB whereas the simulated NF of the die alone has been estimated to 9.5 dB in simulation.

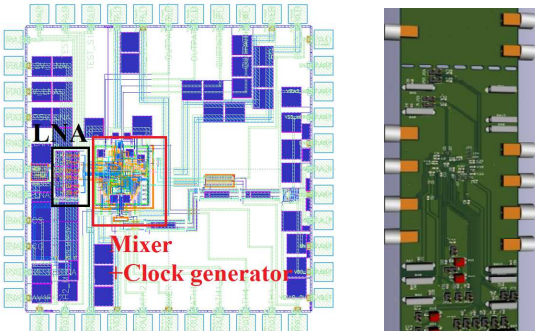

Fig. 10. Layout of the circuit and evaluation board including IF instrumentation amplifiers.

TABLE I. MEASURED POWER CONSUMPTION

Consumption (mW)	LNA	Mixer + CLK - Buff	Total
Measurement	19.6	2.7	22.3

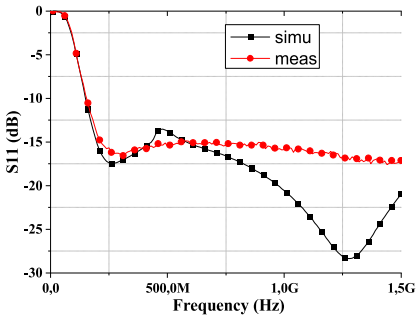

Fig. 11. Measured and simulated S11.

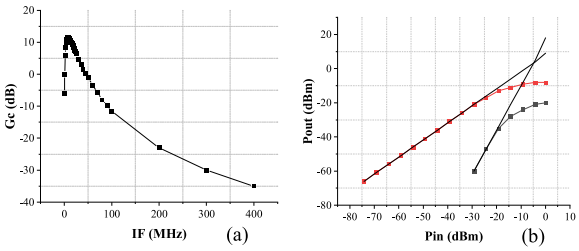

Fig. 12. Measurement: (a) Conversion gain versus IF (b) IIP3.

TABLE II. PERFORMANCE SUMMARY AT f_{RF} = 405 MHz AND f_{IF} = 5 MHz.

Performances	This work	[6]	[5]
Technology	FDSOI 28nm	CMOS 65nm	CMOS 65nm
Frequency (GHz)	0.17–1.2	0.4–0.9	0.2-1
Consumption (mW)*	22**	40***	30**
Conversion gain (dB)	13	34	36
IN-IIP3 (dBm)	-3.5	3.5	/
HRR3 (dB)	46	60	>51
HRR5 (dB)	48	64	>52
HRR7 (dB)	45	-	-
NF (dB)	13.3	4	5.4 - 6

* Excluding clocks, **excluding transimpedance amplifiers TIA, ***Including TIA necessary for harmonics rejection

V. CONCLUSION

An N-Path mixer with harmonic rejection has been designed, implemented and measured for a wide bandwidth of 1:8, that is to say including for the very first time the 7th harmonic while presenting a power consumption comparable to the state of the art HR-8PM. It offers performances in terms of conversion gain of 13 dB and an IB-IIP3 of -3.5 dBm respectively for a power consumption of 22 mW.

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